Curriculum Vitae from Bill Lin

BILL LIN

Associate Dean for Research, Jacobs School of Engineering
Professor, Electrical and Computer Engineering
University of California, San Diego

EDUCATION

1991	Ph.D.	Electrical Engineering and Computer Sciences, University of California, Berkeley
1988	M.S.	Electrical Engineering and Computer Sciences, University of California, Berkeley
1985	B.S.	Electrical Engineering and Computer Sciences, University of California, Berkeley

APPOINTMENTS

2024–present	Associate Dean roles, Jacobs School of Engineering, UC San Diego Associate Dean for Research (2025–present) Associate Dean for Strategic Programs (2024–2025)
2019–2024	Department Chair, Electrical and Computer Engineering, UC San Diego
2017–2019	Department Vice Chair, Electrical and Computer Engineering, UC San Diego
2009–present	Professor, Electrical and Computer Engineering, UC San Diego
1999–2009	Associate Professor, Electrical and Computer Engineering, UC San Diego
1997–1999	Assistant Professor, Electrical and Computer Engineering, UC San Diego
1992–1997	Head of R&D Group, Systems Control and Communications, imec, Leuven, Belgium

LEADERSHIP AND ADMINISTRATIVE EXPERIENCE

Associate Dean for Research and Associate Dean for Strategic Programs, Jacobs School of Engineering (2024–present)

Initially appointed as the Associate Dean for Strategic Programs at the Jacobs School of Engineering, responsible for the research portfolio related to strategic initiatives in microelectronics, computing, and communications. Then became the Associate Dean for Research after one year, responsible for the entire research enterprise spanning the 6 academic departments (Bioengineering, Chemical and Nano Engineering, Computer Science and Engineering, Electrical and Computer Engineering, Mechanical and Aerospace Engineering, and Structural Engineering) and 14 interdisciplinary research centers and institutes at the Jacobs School of Engineering at UC San Diego. In my current role as the Associate Dean for Research, I lead the Jacobs School of Engineering research office that supports about 280 faculty, 130 postdoctoral fellows, 80 research and project scientists, and over 1,350 Ph.D. students and 2,600 MS students, with a diverse research portfolio that currently totals $329 million in annual research expenditures, up 28.5% in the past two years. The Jacobs School of Engineering is ranked #9 among the nation's engineering schools, #2 in the nation in research expenditures per faculty in engineering, and #1 in the nation among public engineering schools for academic papers cited in top 25% of journals.

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Primary Roles and Responsibilities

- Oversee the support of 14 vibrant industry-sponsored interdisciplinary research centers and institutes, each spanning faculty from across multiple engineering departments, many spanning faculty from other parts of campus to go beyond historical, disciplinary boundaries, including the School of Medicine and the School of Biological Sciences on healthcare related engineering research, the School of Physical Sciences on environmental and energy related engineering research, and the School of Social Sciences on society related engineering research, all focusing on high-societal impact challenges.
- Incubate new agile research centers and institutes that become self-supporting in 3 years, with support to attract industry sponsorships and win center-scale grants.
- Responsible for the review and renewal of research centers and institutes and their director reappointments.
- Support large center-scale proposals to federal funding agencies through proposal development support at the Dean's office, in coordination with department-level senior research administrators to form agile proposal development teams.
- Engage and negotiate with outside research development and strategic assessment firms to augment large center-scale proposal development as appropriate.
- Grow the size and diversity of the externally sponsored research portfolio at the Jacobs School, which is currently 47% from industry sponsorship, private gifts, and endowments, 50% from federal grants, and 3% from state funding. This diversified portfolio is robust under the current changing federal funding landscape and uncertainties.
- Work with the Dean to allocate and reallocate space in Franklin Antonio Hall, the Jacobs School's interdisciplinary engineering building.
- Support junior faculty development through working lunches on seeking early career awards and foundation funding opportunities, seed funding for early career award developments, and limited funding to attend agency-specific strategic networking events to build relationships with program managers.
- Work with campus contracts and grants office to negotiate new models of research agreements with government agencies and companies.
- Collaborate with the campus-level Vice Chancellor of Research and Innovation Office on university-level research and innovation committees, including executive task forces on campus-wide AI strategy, cross-school research initiatives and collaborations, and visioning campus priorities.
- Represent the Jacobs School research and partnerships enterprise internally and externally.
- Represent the Jacobs School in international university collaborations.

Contributions to the Dean's Senior Leadership Team

- Participate in the team's meetings every 2 weeks, together with the Dean, Assistant Dean, fellow Associate Deans, and the Executive Director of Development, in which the school's philanthropic strategy, donor cultivation pipeline, and development priorities are discussed, providing direct working knowledge of how a top engineering school's development operation is run.
- Contribute to the Jacobs School's navigation of the campus's current revision of its mission-based resource allocation model, gaining direct working knowledge of the institutional challenges that budget-model transitions pose for schools and their departments.

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- Work with the Dean's senior leadership team and the six department chairs on integrating AI tools into the engineering curriculum and broader learning environment, including the school's development of a Socratic-style AI tutor that connects course material to frontier AI models, and ongoing rethinking of programming instruction and student assessment in the age of AI.

Department Chair, Electrical and Computer Engineering (2019–2024)

I served as Department Chair for 5 years, from 2019 to 2024, leading a department with 65 faculty, 8 of whom were or became members of the National Academy of Engineering during my term, about 25 postdoctoral fellows, 20 research and project scientists, about 350 Ph.D. students, 800 MS students, and 1,350 undergraduate students, with $40 million in annual research expenditures and $37 million in annual core operating budget. I led the department through a period of profound transition, spanning both the pandemic and a generational renewal and expansion of the faculty. That renewal was guided by an ambitious five-year strategic plan I developed through a visioning exercise with all department stakeholders, a blueprint spanning faculty renewal, undergraduate and graduate curricula, teaching innovation, diversity, enrollment planning, and new research initiatives. Over my term, we recruited 18 new faculty, retained all 5 faculty who were actively recruited by competing universities, and facilitated 12 senior faculty retirements, renewing over a quarter of the department while growing it from 59 to 65 faculty, and we navigated the pandemic and post-pandemic disruptions while sustaining the department's $40 million research enterprise undiminished, even though the 12 retiring senior faculty had carried substantial research funding and newly hired junior faculty needed time to build their research programs, positioning the department's next decade of growth. The fruits of this execution were validated externally: in my fourth year, a formal combined undergraduate/graduate program review, conducted by a committee that included senior faculty leaders from Caltech, UC Berkeley, and the University of Washington, examined the department in full, spanning faculty and research, research centers and funding, the graduate and undergraduate programs, staffing, and facilities. The committee unanimously concluded that the department was thriving, with praise across every dimension reviewed and with recommendations framed around sustaining the department's upward trajectory. I implemented all of those recommendations in my final year as Chair.

Key Achievements

Executed an ambitious faculty hiring strategy and a reshaping of the department

- Developed an ambitious new 5-year ECE strategic plan through a visioning exercise engaging all department stakeholders in reimagining every dimension of the department's future: strategic areas for faculty growth and expected retirements; substantial revamping of the undergraduate and graduate curricula to reflect changing industry trends and student interests; new teaching pedagogy and innovations; efforts to increase student and faculty diversity; undergraduate and graduate enrollment planning goals; and opportunities for new inter-departmental and inter-school research centers and initiatives. Then led its execution, reflected in the achievements below.
- Translated the strategy plan into an aggressive expansion of the department with 18 new faculty hires, including 2 senior hires, in areas spanning robotics, machine learning, computer architecture, wireless communications, power systems, photonics, signal processing, and embedded systems. This cohort broadened the department's excellence across fields and backgrounds, including 5 faculty from groups historically underrepresented in engineering.

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- Among the 18 new faculty recruited during my term, they have collectively won over 25 major new awards and distinctions since joining UC San Diego, including a new senior faculty inducted into the National Academy of Engineering and winning the IEEE/RSE James Clerk Maxwell Medal, new junior faculty winning four NSF CAREER awards, the DARPA Young Faculty Award, the ONR Young Investigator Award, the Beckman Young Investigator Award, the NIH Trailblazer Awards, the ISIF Young Investigator Awards, the Sloan Research Fellowship, the Kavli Fellow of the National Academy of Sciences award, and new junior faculty winning major prizes, including two Donald P. Eckman Awards, and the Vasil A. Popov Prize. I trace these successes directly to the new junior-faculty success initiatives described below: the revamped faculty mentoring program, the Senior Faculty to Junior Faculty Lunch series, and the faculty-only research-visions seminar series, among others.
- Made 3 of the 18 new hires as joint appointments with campus units beyond the Jacobs School of Engineering: the Scripps Institution of Oceanography, the new School of Computing, Information, and Data Science, and the UC San Diego Design Lab, an independent interdisciplinary unit spanning faculty from the Schools of Medicine, Social Sciences, Arts and Humanities, Public Health and Human Longevity Science, and Business. These joint hires advanced my objective as Chair of seeding interdisciplinary research collaborations and centers beyond the School of Engineering.
- Negotiated, together with the Dean and fellow engineering department chairs, a new funding model for faculty hiring based on revenue generated from the Master's program, and transitioned the department to it, in part enabling the transformative growth. This model exemplifies diversifying core revenues through professional master's programs. Five of the 18 new hires, including two senior hires and three faculty from groups historically underrepresented in engineering, were funded directly through this model; together, these five have won 12 major awards and prizes since joining UC San Diego.
- Oversaw the promotion and tenure of more than a dozen faculty.
- Facilitated 12 senior faculty retirements.
- Retained 100% of faculty facing recruitment by other institutions: personally negotiated successful retention offers in all 5 retention cases that arose during my 5-year term, keeping each faculty member at UC San Diego. All 5 were senior faculty who ranked among the department's most highly funded, most awarded, and most highly cited, with among its most extensive laboratories, and two were research center directors. Each retention was won in large part by making the case that they were highly valued and that their careers would flourish at UC San Diego, not by compensation alone.

Launched new initiatives to support junior faculty success

- Revamped the ECE faculty mentoring program by pairing every junior faculty with a senior faculty mentor, with the senior faculty committed to their success. Worked with the Dean's office to create a new annual faculty mentoring award formally recognizing the mentoring of a senior faculty to a junior faculty.
- Launched a new monthly "Senior Faculty to Junior Faculty Lunch series," with a senior faculty holding a conversation each time on a different topic relevant to the success of junior faculty, including how to develop relationships with program managers and companies, how to identify, attract and nurture top students, and how to identify and develop high-impact research agendas.

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- Launched a new bi-quarterly faculty-only seminar series for junior faculty to share their research visions with senior faculty as a vehicle to foster new collaborations between our new faculty and the rest of the department.
- Launched a new repository of successful NSF CAREER and Young Investigator Award proposals as references for junior faculty to go after the same programs, with the faculty providing the proposal samples serving as mentors.
- Launched a mentored seed funding program based on a generous gift that pairs an assistant professor with a senior faculty to develop new collaborations, with commitments from the recipients to submit a joint-proposal to an external funding agency within one year.

Established new initiatives on teaching innovations and advancing the teaching mission

- Doubled the number of faculty in the "Teaching Professor" series, as part of the new faculty hirings, who are tenure-track faculty focused primarily on undergraduate teaching, curriculum design, and pedagogy.
- Launched a new "Teaching Innovations" standing committee, initially launched in response to the pandemic to develop and share remote classroom methods and best practices. The committee, comprising all faculty in the teaching professor series and regular ladder-rank faculty, continued to develop and share new teaching innovations on an ongoing basis post-pandemic, including new evidence-based, learner-centered, and equitable teaching practices.
- Launched a new faculty-only quarterly "Teaching Innovations Seminar" series in which teaching leaders on our faculty, as well as external teaching leaders, share teaching innovations and practices.
- Served on the UC San Diego campus-wide executive task force on "Holistic Teaching Evaluation," representing a profound shift in how the university defines, measures, and rewards effective teaching in academic reviews. The new model encourages critical self-reflection, actionable pedagogical strategies and student learning, and inclusive pedagogy in genuine efforts toward student success.

Expanded curriculum and student engagements

- Expanded our hands-on curriculum throughout our undergraduate program to make use of the new 3,000-square-foot Envision Arts and Engineering Maker Studio at UC San Diego.
- Created a new undergraduate depth in power systems and power engineering.
- Led a major revision to the Computer Engineering curriculum.
- Led the department through a highly-successful formal combined undergraduate/graduate program review with external reviewers. The review committee gave strong praise to our innovative teaching and learning methods, and to our vibrant student community. This extensive external review was conducted toward the end of my term, reflecting the significant progress the department had made. The committee further recommended that the department be nominated for the ECEDHA Innovative Program Award, which the department went on to win in March 2024, in my final year as Chair.
- Led the department through a major ABET accreditation review early in my term.
- Launched a new ECE Alumni Mentoring Program with over 100 ECE alumni mentoring over 150 undergraduate students, providing guidance on career paths and life after graduation. Greatly increased alumni engagement in the process.
- Partnered with the campus development team to secure and steward a $2.4 million donor gift supporting ECE Ph.D. fellowships.

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- Collaborated closely with both undergraduate and graduate student organizations in organizing events and workshops, including the signature annual ECE Day where the student organizations showcase their achievements, and the annual HARD Hack event, San Diego's largest hardware-focused hackathon competition.
- Championed a thriving student-organization community whose achievements earned national recognition, including the UC San Diego chapter of IEEE-Eta Kappa Nu winning the IEEE-HKN Outstanding Chapter Award in each of the five years of my Chair term.

Strengthened the department leadership structure

- Reimagined and expanded the ECE Faculty Council into a broadly representative, deliberative body where the department's hardest questions were vetted before decisions were made, giving faculty a real stake in our outcomes and giving me candid counsel through a demanding period.
- Created new department committees and broadened committee chair leadership authorities and responsibilities.
- Substantially revised the faculty academic review process.

Led ECE through the pandemic and post-pandemic transition

- Maintained research continuity across the department's research enterprise: implemented laboratory ramp-down/ramp-up protocols, and protected doctoral students' funding and degree progress through prolonged disruption.
- Directed the transition of all faculty, lecturers, teaching assistants, and approximately 1,350 undergraduate and 1,150 graduate students to remote instruction, rapidly standing up teaching resources and support for both instructors and students, and led the subsequent return-to-campus transition.
- Transitioned 40+ staff across 6 functional areas to remote operations, then to hybrid schedules, sustaining department services without interruption.
- Translated evolving campus policy into concrete departmental guidance and protocols throughout.
- Concurrently executed the department's migration to the campus's new ESR Oracle financial system, despite pandemic constraints.
- Navigated the department's budget and operations through the campus's then-new mission-based resource allocation model, amid pandemic-era financial uncertainty.

Vice Chair, Electrical and Computer Engineering (2017–2019)

- Led undergraduate committee responsible for undergraduate curricular and programmatic policies.
- Led graduate committee responsible for graduate curricular and programmatic policies.
- Responsible for student petitions and student matters.

Principal Investigator, EMPOWER Program, Jacobs School of Engineering (2022–present)

I serve as Principal Investigator of EMPOWER, a $5 million, school-wide student success initiative funded by the National Science Foundation's S-STEM program (2022–2027). EMPOWER supports talented, low-income community college transfer students across all 6 engineering departments at the Jacobs School, in partnership with Southwestern College and Imperial Valley College, providing

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scholarships together with a structured program of high-impact practices: enrichment and professional development workshops, multi-dimensional faculty and alumni mentoring, summer internship preparation, undergraduate research experiences, and community-building activities that foster a sense of belonging, designed to address the distinct challenges of transitioning from two-year to four-year institutions and into engineering careers. To date, the program has served 240 scholars across 4 cohorts at the 3 partner institutions, a population that is predominantly first-generation, nearly half women, and predominantly from groups historically underrepresented in engineering.

- Lead a team of 4 co-PIs, directing the program's design, execution, and continuous assessment.
- Direct the program's evaluation and research component: program evaluation shows scholars reporting high motivation and sense of belonging (averaging above 5 on 7-point validated scales, with career motivation highest among all measured factors), with program design and findings published in 5 peer-reviewed engineering education studies at the American Society for Engineering Education (ASEE) Annual Conference.
- Coordinate scholar recruitment and selection at UC San Diego, awarding need-based scholarships of up to $10,000 per scholar.
- Build and sustain cross-institutional partnerships with the 2 community colleges, including semi-annual campus visit days engaging prospective transfer students in the pathway to four-year engineering programs.
- Connect scholars to research experiences with faculty across all 6 engineering departments and to structured multi-week internship preparation with industry placement support.

UNIVERSITY SERVICE AND SHARED GOVERNANCE

University Level, UC San Diego

Member, Search Committee for Executive Vice Chancellor (appointed by the Chancellor), 2026

Member, Search Committee for Senior Associate Vice Chancellor of Research Innovation, 2026

Member, Search Review Panel, Director of Research Development, Office of Research and Innovation, 2026

Member, AI Strategy Committee, Office of Research and Innovation, 2024–2025

Member, Holistic Teaching Evaluation Oversight Committee, 2022–2023

Member, Task Force on the Formation of the School of Computing, Information, and Data Science, 2021–2022

Member, Advisory Council on Equity, Diversity, and Inclusion, 2021–2022

Member, Council of Undergraduate Education, 2017–2019

Member, Search Committee for Associate Vice Chancellor of Innovation and Industry Alliances, 2011–2012

School Level, Jacobs School of Engineering

Chair, Jacobs School Strategic Planning Committee on Diversity & Culture of Inclusion, 2019–2020

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Member, Franklin Antonio Hall Building Committee (space programming and laboratory design with project architects), 2018–2019

Selected Department Level, Electrical and Computer Engineering

Member, ECE Faculty Council (advisory council to the Department Chair), 2016–2019, 2024–present

Member, ECE Academic Personnel Committee, 2024–2025

Chair, ECE Computer Engineering Graduate Curriculum Council, 2024–2025

Chair, ECE Software Curriculum Committee, 2018–2019

Chair, ECE Undergraduate Student Affairs Committee, 2010–2011, 2016–2019

Chair, ECE Faculty Search Committee, 2016–2017

TEACHING EXPERIENCE

1. ECE 5, *Experience ECE Making, Breaking, Hacking Stuff* (undergraduate level)
   Spring 2024, Spring 2022.
   An introduction to electrical and computer engineering via "hands-on" projects in circuits, signal processing, robotics and control, and embedded systems, culminating in a team competition on designing the control software to "self-drive" a robot car through racetracks.

2. ECE 284, *Special Topics in Computer Engineering* (graduate level)
   Spring 2022, Spring 2013, Spring 2012.
   Topics taught in this graduate-level special topics course include hardware accelerators and distributed systems for networking, wireless communications, and most recently artificial intelligence.

3. ECE 111, *Advanced Digital Design Project* (undergraduate level)
   Winter 2019, Spring 2018, Winter 2018, Spring 2017, Winter 2017, Fall 2016, Winter 2016, Winter 2015, Fall 2015, Spring 2014, Spring 2013, Spring 2012, Spring 2011, Spring 2010, and other quarters before 2010.
   Large-scale senior capstone design project course on designing application-specific hardware accelerators for different applications, from wireless packet processing, encryption and decryption, to cryptocurrency mining. Students learn Verilog-based synthesis flows for rapid prototyping to FPGAs using design automation, timing and power analysis, and simulation tools.

4. ECE 25, *Introduction to Digital Design* (undergraduate level)
   Fall 2014, Winter 2014, Fall 2012, Spring 2012, Fall 2010, and other quarters before 2010.
   Lower-division course covering digital logic design, including Boolean algebra, combination and sequential logic, gates and their implementation in digital circuits. Principles introduced in lectures are used in laboratory assignments, which also serve to introduce experimental and design methods.

5. CSE 140, *Components and Design Techniques for Digital Systems* (undergraduate level)
   Fall 2011.
   Upper-division course covering Boolean logic and finite state machines; two-level, multilevel combinational logic design, combinational modules and modular networks, Mealy and Moore machines, analysis and synthesis of canonical forms, sequential modules.

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6. CSE 140L, *Digital Systems Laboratories* (undergraduate level)
   Fall 2011.
   Upper-division companion lab course covering implementation with computer-aided design tools for combinational logic minimization and state machine synthesis.
7. ECE 260A, *VLSI Digital System Algorithms and Architectures* (graduate level)
   Taught before 2010.
   Custom and semicustom VLSI design from both the circuit and system designer's perspective. MOS transistor theory, circuit characterization, and performance estimation. CMOS logic design will be emphasized.
8. ECE 260C, *VLSI Advanced Topics* (graduate level)
   Taught before 2010.
   Advanced topics in design practices and methodologies for modern system-on-chip design. Different design alternatives are introduced and analyzed. Advanced design tools are used to design a hardware-software system.
9. CSE 291, *Application Specific Processors* (graduate level)
   Taught before 2010.
   Graduate level computer architecture course focused on contemporary processor architectures aimed at special-purpose high-speed functions.
10. ECE 20B, *Introduction to Electrical Engineering II* (undergraduate level)
    Taught before 2010.
    Introduction to electrical engineering.

STUDENT ADVISING

Current Graduate Students

1. Emma Dunmire
2. Aarav Vidhawan
3. April Hsu
4. Kaila Rosing (co-advisor with Prof. F. Ponzina at SDSU)
5. Yucheng Wang (collaboration with Prof. C.K. Cheng)
6. Byeonggon Kang (collaboration with Prof. C.K. Cheng)

Ph.D. Students Supervised or Co-Advised

1. Litao Qiao, *Learning and Explaining Decision Rules for Tabular Data: A Boolean Logic Approach*, Ph.D. 2026 (Wayfair R&D Division)
2. Mahdi Morafah, *Advancing Federated Learning for Heterogeneous and Non-IID Data in Edge Intelligence Environments*, Ph.D. 2025 (Postdoctoral Fellow at Wharton Business School, University of Pennsylvania)

3. Saeed Vahidian, *On Distributed Learning Techniques for Machine Learning*, Ph.D. 2023 (Assistant Professor of Electrical and Computer Engineering at Oklahoma State University)
4. Weijia Wang, *Efficient and Explainable Machine Learning*, Ph.D. 2023 (Walmart Global Tech)
5. Uday Mallappa, *AI for Design Optimization and Design for AI Acceleration*, Ph.D. 2023, thesis co-chair with Prof. C. K. Cheng (Intel)
6. Chia-Tung Ho, *Novel Computer Aided Design (CAD) Methodology for Emerging Technologies to Fight the Stagnation of Moore's Law*, Ph.D. 2022, thesis co-chair with Prof. C. K. Cheng (NVIDIA)
7. Daeyeal Lee, *Logical Reasoning Techniques for VLSI Applications*, Ph.D. 2022, thesis co-chair with Prof. C. K. Cheng (Samsung)
8. Dongwon Park, *Logical Reasoning Techniques for Physical Layout in Deep Nanometer Technologies*, Ph.D. 2021, thesis co-chair with Prof. C. K. Cheng (Qualcomm)
9. Ping Yin, *Destination-based Routing and Circuit Allocation for Future Traffic Growth*, Ph.D. 2020 (Meta)
10. Yang Song, *On Quality-of-Service and Memory Efficiency in Heterogeneous MPSoCs*, Ph.D. 2019 (NVIDIA)
11. Yashar Asgarieh, *Making the On-Chip World Smaller with Low-Latency On-Chip Networks*, Ph.D. 2018 (NVIDIA)
12. Hao Wang, *Designing Network Traffic Managers with Throughput, Fairness, and Worst-case Performance Guarantees*, Ph.D. 2011 (Oracle)
13. Chia-Wei Chang, *Efficient Gain-Driven Routing-Assisted Mechanisms for Network-Wide Traffic Monitoring*, Ph.D. 2011 (Qualcomm)
14. Rohit Sunkam Ramanujam, *Throughput-driven Design of Networks-on-Chip*, Ph.D. 2011 (Juniper Networks)
15. Jerry Chou, *A New Network Architecture for Future Optical Networks: Coarse Optical Circuit Switching by Default, Rerouting over Circuits for Adaptation*, Ph.D. 2009 (Professor of Computer Science at the National Tsing Hua University, Taiwan)
16. Shan Yan, *Synthesis of Application-Specific On-Chip Networks*, Ph.D. 2009 (Broadcom)
17. Steven Vercauteren, Ph.D. 1998 from imec, co-led research with Prof. Hugo De Man (European Patent Office)
18. Eric Verlind, Ph.D. 1996 from imec, co-led research with Prof. Hugo De Man (Proximus)
19. Tilman Kolks, Ph.D. 1996 from imec, co-led research with Prof. Hugo De Man (co-founder Buus)
20. Milton Sawasaki, Ph.D. 1994 from imec, co-led research with Prof. Hugo De Man
21. Peter Vanbekbergen, Ph.D. 1993 from imec, co-led research with Prof. Hugo De Man (partner & co-founder imec.xpand)

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M.S. Students Supervised

1. Sunreet Khanna (2025–2026, MS research advisor))
2. Abhishikta Panja (2024, MS research advisor)
3. Reya Sadhu (2024, MS research advisor)
4. Sree Bhargavi Balija (2023, MS research advisor)
5. Debalina Chowdhury (2023, MS research advisor)
6. Sreevatsank Kadaveru (2022–2023, MS research advisor)
7. Woonjoon Baek (2022–2023, MS research advisor)
8. Eric Zhang (2019, MS research advisor)
9. Jianing Zhang (2019–2020, MS research advisor)
10. Kewei Xu (2018–2019, MS research advisor)
11. Siddhartha Saha (2006, MS research advisor)
12. Chris Roedel (2005, MS research advisor)
13. Michael Roeder (2005, MS research advisor)
14. Sumeet Swaroop (2005, MS research advisor)
15. Vikas Motwanti (2005, MS research advisor)
16. Xiaohan Zhu (1999, MS research advisor)

Undergraduate Students Supervised

1. Shengqi Wu (2025–2026, undergraduate research advisor)
2. Kevin Liang (2025–2026, undergraduate research advisor)
3. Lilian Kong (2024–2025, undergraduate research co-advisor with Prof. Cheng)
4. Hojin Chang (2023–2024, undergraduate research advisor)
5. Zichen Zhou (2022, undergraduate research co-advisor with Prof. Cheng)
6. Nihal Nazeem (2022, undergraduate research co-advisor with Prof. Cheng)
7. Benny Cai (2022, undergraduate research advisor)
8. Aoxi Li (2022, undergraduate research co-advisor with Prof. Cheng)
9. Stephen Kim (2021, undergraduate research advisor)
10. Jeremiah Fong (2012, undergraduate research advisor)
11. William Grant (2010, undergraduate research advisor)

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12. Michael Tartre (2007–2008, undergraduate research advisor)
13. Andrew May (1999, undergraduate research advisor)
14. James Hurt (1999, undergraduate research advisor)

Visiting Scientists

Guang Sun (2011–2022, visiting scientist from Tsinghua University, Beijing)

Doctoral Dissertation Committees

Served on 80+ Doctoral Dissertation Committees in ECE and CSE at UC San Diego

HONORS AND RECOGNITIONS

Innovative Program Award, Electrical and Computer Engineering Department Heads Association (ECEDHA), awarded to the UC San Diego ECE Department during my term as Chair (2024)

Jacobs Faculty Scholar

Hellman Fellow

Hughes Fellow

Best Paper Award Nomination, ACM/IEEE Design Automation Conference (2012)

Best Paper Award Nomination, Design Automation and Test in Europe Conference (1998)

Best Paper Award, IEEE Transactions on VLSI Systems (1995)

Best Paper Award Nomination, ACM/IEEE Design Automation Conference (1994)

Distinguished Paper Citation, IEEE International Conference on Computer-Aided Design (1990)

Distinguished Paper Citation, IFIP International Conference on VLSI (1989)

Best Paper Award, ACM/IEEE Design Automation Conference (1987)

Eta Kappa Nu

Tau Beta Pi

FUNDED GRANTS, GIFTS AND PROJECTS

1. “Agentic-AI for mmWave RFIC Design with Human-in-the-Loop,” $45,000, Center for Wireless Communications, UC San Diego (industry consortium–sponsored), Principal Investigator (with 1 co-PI), 2026–2027.
2. “Economics and Application-Aware AI-on-RAN: Co-optimizing Wireless Capacity and AI Compute under Real-time Constraints,” $45,000, Center for Wireless Communications, UC San Diego (industry consortium–sponsored), Principal Investigator (with 1 co-PI), 2026–2027.

3. “Monolithic Silicon-Photonics Accelerators Enabling Next-Gen Extreme MIMO,” $540,000, National Science Foundation, Co-Principal Investigator (with 2 other co-PIs), 2024–2027.
4. “Monolithic Silicon-Photonics Accelerators Enabling Next-Generation Extreme MIMO,” $100,000, Center for Wireless Communications, UC San Diego (industry consortium–sponsored), Principal Investigator, 2024–2026.
5. “Large Scale Federated Learning Over a Huge Diversity of Devices in Next-Generation 5G/6G Edge Computing Environments,” $85,000, Center for Wireless Communications, UC San Diego (industry consortium–sponsored), Principal Investigator (with 1 co-PI), 2024–2026.
6. “Monolithic Silicon-Photonics Accelerators for Large Language Models at the Speed of Light,” $40,000, ECE Seed Grant, Co-Principal Investigator (with 1 other co-PI), 2024–2025.
7. “Large Scale Federated Learning Over a Huge Diversity of Devices in Next-Generation Edge Computing Environments,” $200,000, Cisco, Principal Investigator, 2023–2024.
8. “From Promise to Reality: Empowering Low-Income Students through High Impact Practices to Achieve Academic and Professional Success in Engineering,” $5,000,000, National Science Foundation, Principal Investigator (with 4 co-PIs), 2022–2027.
9. “Exchanging Knowledge Beyond Data Between Human and Machine Learner,” $500,000, National Science Foundation, Principal Investigator (with 1 co-PI), 2020–2024.
10. “Deep Reinforcement Learning for Robot Planning,” $50,000, ECE Seed Grant, Co-Principal Investigator (with 1 other co-PI), 2018–2019.
11. Research Gift in Support of Heterogeneous Systems-on-Chip Research, $50,000, Qualcomm, 2017.
12. “Research into Worst-Case Large Deviation Theory for Network Algorithmics,” $250,000, National Science Foundation, Principal Investigator, 2014–2017.
13. Research Gift in Support of Application-Specific Processor Research, $75,000, Qualcomm, 2014.
14. “A New Methodology for Advanced Semiconductor Manufacturing and Data Center Networking,” $750,000, National Science Foundation, Principal Investigator, 2012–2016.
15. “Research on Architecture-Level Estimation and Optimization for Networks-On-Chip Building Blocks,” $450,000, National Science Foundation, Co-Principal Investigator (with 1 other co-PI), 2011–2014.
16. “Towards Versatile and Programmable Measurement Architecture for Future Networks,” $200,000, National Science Foundation, Principal Investigator, 2009–2012.
17. “Wireless Cloud Computing for Thin Clients,” $200,600, Industry-University Cooperative Research Program (IUCRP), Co-Principal Investigator (with 3 co-PIs), 2009–2011.
18. “Enabling Personalized, Context Aware, and Interactive Mobile Advertisements,” $278,800, IUCRP, Co-Principal Investigator (with 3 co-PIs), 2009–2011.
19. “High-Throughput Router Microarchitectures for On-Chip Interconnection Networks,” $14,310, UC San Diego Academic Senate, Principal Investigator, 2009–2010.

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20. "Can Coarse Circuit Switching Work and What to Do When it Doesn't?" $86,400, Qualcomm, HP, Sun (industry consortium), Principal Investigator, 2008–2010.
21. Research Gift in Support of Internet Measurement Research, $40,000, AT&T, 2008.
22. "Proactive Surge Protection," $15,000, UC San Diego Academic Senate, Principal Investigator, 2008.
23. "Application of Coding to the Internet Backbone," $130,000, AT&T, Qualcomm, HP, Sun (industry consortium), Principal Investigator (with 1 co-PI), 2006–2008.
24. "Mapping Applications to a Distributed Embedded Processor Architecture," $41,977, UC MICRO, Principal Investigator, 2006–2007.
25. "Towards a More Fair and Robust Internet Backbone," $180,000, AT&T, Qualcomm, HP, Sun (industry consortium), Principal Investigator (with 2 co-PIs), 2005–2007.
26. "Scalable Video for Wireless Communications," $495,274, UC Communications Research Program (UC CoRe), Principal Investigator (with 3 co-PIs), 2005–2007.
27. Research Gift in Support of Microelectronics Research, $15,000, ST Microelectronics, 2005.
28. "Network-on-Silicon Architectures for Mesh-Based Radios," $148,400, Nokia, Ericsson, Texas Instruments, Skyworks (industry consortium), Principal Investigator, 2003–2005.
29. "Traffic Analysis for Design of Multimedia Applications," $140,000, ST Microelectronics, Principal Investigator, 2003–2004.
30. "Configurable Platform Architectures and Applications for Ubiquitous Wireless Communications," $315,800, IUCRP, Co-Principal Investigator (with 3 co-PIs), 2001–2003.
31. "In-Home Ad-Hoc Networks," $233,238, IUCRP, Co-Principal Investigator (with 4 co-PIs), 1999–2000.
32. "Single-Chip Radio Transceivers," $333,575, IUCRP, Co-Principal Investigator (with 2 co-PIs), 1999–2000.
33. "Wireless Access to the Internet," $297,981, IUCRP, Co-Principal Investigator (with 4 co-PIs), 1999–2000.
34. "Space-Time Processing for Mobile Communication," $255,698, IUCRP, Co-Principal Investigator (with 4 co-PIs), 1999–2000.
35. "A Systems Approach to Wireless ATM," $900,000, Sprint, Co-Principal Investigator (with 4 co-PIs), 1997–2000.

PROFESSIONAL CONTRIBUTIONS

Editorial Work

Associate Editor, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2012–2015.

Guest Editor, *IEEE Transactions on Network and Service Management (TNSM)*, 2012

Editorial Board, *International Journal of Embedded Systems*, 2003–2013

Conference Organizing Committees

General Chair, *ACM SIGMETRICS*, 2015

General Chair, *ACM/IEEE International Workshop on Quality-of-Service (IWQoS)*, 2011

General Chair, *ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS)*, 2010

General Chair, *ACM/IEEE Symposium on Networks-on-Chips (NOCS)*, 2009

Steering Committees, *ACM/IEEE International Workshop on Quality-of-Service (IWQoS)*, 2012–2015

Steering Committees, *ACM/IEEE Symposium on Architecture for Networking and Communications Systems (ANCS)*, 2010–2022

Steering Committees, *ACM/IEEE Symposium on Networks-on-Chips (NOCS)*, 2009–2023

Chair of Steering Committee, *ACM/IEEE Symposium on Architectures for Networking & Communications Systems (ANCS)*, 2013–2015

Industrial Chair, *ACM/IEEE Symposium on Networks-on-Chips (NOCS)*, 2010

Posters Chair, *ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS)*, 2009

Special Session Organizer, *International Symposium on Circuits and Systems (ISCAS)*, 2005

Topic Co-Chair, *Design Automation and Test in Europe Conference (DATE)*, 2000

Tutorials Chair, *International Symposium on Asynchronous Circuits and Systems (ASYNC)*, 1998

Special Hot-Topics Session Organizer, *European Design and Test Conference (ED&T)*, 1996

Technical Program Committees

ACM/IEEE Design Automation Conference (DAC), 2012–2014, 1996.

IEEE Conference on Computer Communications (INFOCOM), Work-In-Progress Track, 2010.

Design Automation and Test in Europe Conference (DATE), 2009–2010, 2000.

IEEE International Conference on Computer Design (ICCD), 2009.

ACM/IEEE Symposium on Architectures for Networking & Comm. Systems (ANCS), 2008–2012.

IEEE International Conference on Network Protocols (ICNP), 2008.

ACM/IEEE Symposium on Networks-on-Chips (NOCS), 2007–2012.

IEEE Symposium on High Performance Interconnects (HOTI), 2007–2010.

IEEE GLOBECOM, 2006.

Asia Pacific Hardware Description Languages Conference (APCHDL), 1998, 1993–1994.

European Design and Test Conference (ED&T), 1995–1996.

IFIP Working Conference on Logic and Architecture Synthesis, 1995.

International Symposium on Asynchronous Circuits and Systems (ASYNC), 1994–1999.

IFIP Working Conference on Logic and Architecture Synthesis, 1993–1994.

European Conference on Design Automation (EuroDAC), 1993–1994.

PROFESSIONAL MEMBERSHIPS

Institute of Electrical and Electronics Engineers (IEEE)

Association for Computing Machinery (ACM)

KEYNOTES, INVITED TALKS, AND PANELS (12)

[L1] "The Cutting Edge of Advanced Microelectronics and Semiconductors," *Competitiveness Conversations Across America: Building the Next Economy's Strategic Innovation Stack–Compute, AI, Energy, Bio, Autonomy, and Security*, San Diego, July 2026. **Invited Talk.**

[L2] "Growing the Greater SD Semiconductor Ecosystem," *Center for Strategic and International Studies*, San Diego, October 2025. **Panelist.**

[L3] "Optical Circuit Switching by Default, Indirect Routing over Circuits for Adaptation," *International Workshop on Mathematical Issues in Information Sciences (MIIS)*, Shenzhen, China, December 2017. **Invited Talk.**

[L4] "Dark Fiber Meets Dark Silicon," *IEEE International Performance, Computing and Communications Conference*, San Diego, CA, December 2013. **Keynote Talk**.

[L5] "Can You Hear Me Now? On-Chip Communication in the Thousand Core Era," *IEEE Green Computing Conference, Lighter-than-Green Dependable Multicore Architectures Workshop*, San Jose, CA, June 2012. **Keynote Talk**.

[L6] "Design Technology for Embedded Computing," *The 5th Asia Pacific Conference on Hardware Description Languages*, Seoul, Korea, July 1998. **Invited Talk.**

[L7] "Representation Issues in Co-Design," *The 4th ACM/IEEE International Workshop on Hardware/Software Co-design*, Pittsburgh, PA, March 1996. **Panelist.**

[L8] "Broadband Telecom System Design," *European Design and Test Conference*, Paris, France, March 1996. **Panelist.**

[L9] "ASICs in China," *The 2nd International Conference on ASIC*, Shanghai, China, October 1996. **Panelist.**

[L10] "Designing Single-Chip Systems," *The 2nd International Conference on ASIC*, Shanghai, China, October 1996. **Invited Talk.**

[L11] "Are Cores a Serious Business?" *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 1995. **Panelist.**

[L12] "Design of Heterogeneous ICs for Mobile and Personal Communication Systems," IEEE International Conference on Computer-Aided Design, San Jose, CA, November 1994. **Invited Talk.**

PATENTS ISSUED (6)

[P1] United States Patent 12,374,394, issued July 2025. Title: "*Degradation-Aware Training Scheme for Reliable Memristor Deep Learning Accelerator Design*." Inventors: D. Dang, D. Sahoo, **B. Lin**, R. Mahapatra, A. Khansama, and S. Govardan.

[P2] United States Patent 8,443,444, issued May 2013. Title: "*Mitigating Low-Rate Denial-Of-Service Attacks in Packet-Switched Networks*." Inventors: J. Wang, C.-W. Chang, S. Lee, **B. Lin**.

[P3] United States Patent 7,860,004, issued December 2010. Title: "*Systems and Methods for Proactive Surge Protection*." Inventors: O. Spatscheck, S. Sen, **B. Lin**, J. Chou.

[P4] United States Patent 7,672,005, issued March 2010. Title: "*Method and Apparatus for Scan Block Caching*." Inventors: D. V. Hobbs, **B. Lin**.

[P5] United States Patent 5,870,588, issued February 1999. Title: "*Design Environment and a Design Method for Hardware/Software Co-Design*." Inventors: K. Van Rompaey, D. Verkest, J. Vanhoof, **B. Lin**, I. Bolsens, H. De Man.

[P6] United States Patent 5,748,487, issued May 1998. Title: "*System and Method for Generating a Hazard-Free Asynchronous Circuit*." Inventors: M.H. Sawasaki, C. Ykman-Couvreur, **B. Lin**, H. De Man.

BOOK CHAPTERS (6)

[B1] S. Yan and **B. Lin**, "Design of Application-Specific 3D Networks-on-Chip Architectures," in *3D Integration for NoC-based SoC Architectures*, Springer, 2011, pp. 167-191.

[B2] H. De Man, I. Bolsens, **B. Lin**, K. Van Rompaey, S. Vercauteren, and D. Verkest, "Co-Design of DSP Systems," in *Hardware/Software Co-design*, Kluwer Academic Publishing, 1996, pp. 75-104.

[B3] T. Kolks, **B. Lin**, and H. De Man, "Sizing of Communication Buffers for Communicating Signal Processors," in *VLSI Signal Processing VI*, New York: IEEE Press, 1993, pp. 426-434.

[B4] **B. Lin** and A.R. Newton, "Exact Redundant State Registers Removal based on Binary Decision Diagrams," in *Very Large Scale Integration*, Amsterdam: Elsevier Science Publishers B.V. and North Holland Press, 1992, pp. 277-286.

[B5] **B. Lin**, G.S. Whitcomb, and A.R. Newton, "Symbolic Don't Cares and Equivalence in High-Level Synthesis," in *Logic and Architectural Synthesis*, Amsterdam: Elsevier Science Publishers B.V. and North Holland Press, 1991, pp. 19-27.

[B6] **B. Lin** and A.R. Newton, "Synthesis of Multiple Level Logic from Symbolic High-Level Description Languages," in *Very Large Scale Integration*, Amsterdam: Elsevier Science Publishers, B.V. and North Holland Press, 1990, pp. 187-196.

JOURNAL PUBLICATIONS (87)

[J1] K. Liang, L. Qiao, I. Keslassy and **B. Lin**, "Scheduling Parallel Optical Switches in Datacenters," *IEEE Networking Letters*, vol. 8, pp. 149-153, 2026.

[J2] S. Chaudhury, K. Johnson, N. Alic, **B. Lin**, Y. Fainman, and T.C. Hsueh, "Monolithic Silicon-Photonics Sign-Sign Dot-Product Circuits Toward Artificial Intelligence and Multiple-Input Multiple-Output Accelerators," *Nanophotonics*, vol. 15, no. 8, p.e70063, 2026.

[J3] T.C. Hsueh, **B. Lin**, Z. Chen, and Y. Fainman, "Panel-Scale Reconfigurable Photonic Interconnects for Scalable AI Computation," *IEEE Open Journal of the Solid-State Circuits Society*, 2025.

[J4] M. Morafah, H. Chang, C. Chen and **B. Lin**, "Federated Learning Client Pruning for Noisy Labels," *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*, vol. 10, no. 2, pp. 8:1-8:25, 2025.

[J5] S. Chaudhury, K. Johnson, V. Fedorov, **B. Lin**, Y. Fainman and T.-C. Hsueh, "Micro-Ring Modulator Linearity Enhancement for Analog and Digital Optical Links," *IEEE Photonics Technology Letters*, vol. 36, no. 4, 1457-1460, 2024.

[J6] T.-C. Hsueh, Y. Fainman, and **B. Lin**, "Monolithic Silicon-Photonics Linear-Algebra Accelerators Enabling Next-Gen Massive MIMO," *Journal of Lightwave Technology*, vol. 42, no. 22, 7903-7918, 2024.

[J7] T.-C. Hsueh, Y. Fainman, and **B. Lin**, "Optical Comb-Based Monolithic Photonic-Electronic Accelerators for Self-Attention Computation," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 30, no. 5, 2024.

[J8] S. Vahidian, M. Morafah, C. Chen, M. Shah and **B. Lin**, "Rethinking Data Heterogeneity in Federated Learning: Introducing a New Notion and Standard Benchmarks," *IEEE Transactions on Artificial Intelligence*, vol. 5, no. 3, pp. 1386-1397, 2024.

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[J13] L. Qiao, W. Wang and **B. Lin**, "Alternative Formulations of Decision Rule Learning from Neural Networks," *Machine Learning and Knowledge Extraction*, vol. 5, no. 3, pp. 937-956, 2023.

[J14] C.-K. Cheng, C. Holtz, A. B. Kahng, **B. Lin** and U. Mallappa, "DAGSizer: A Directed Graph Convolutional Network Approach to Discrete Gate Sizing of VLSI Graphs," *ACM Transactions on Design Automation of Electronic Systems*, vol. 28, no. 4, pp. 52:1-52:31, 2023.

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[J16] S. Vahidian, M. Joneidi, A. Esmaeili, S. Khodadadeh, S. Zehtabian and **B. Lin**, "Spectrum Pursuit With Residual Descent for Column Subset Selection Problem: Theoretical Guarantees and Applications in Deep Learning," *IEEE Access*, vol. 10, pp. 88164-88177, 2022.

[J17] W. Wang, L. Qiao, and **B. Lin**, "Tabular Machine Learning using Conjunctive Threshold Neural Networks," *Machine Learning with Applications*, Elsevier, p.100429, 2022.

[J18] S.F. Hafshejani, S. Vahidian, Z. Moaberfard, and **B. Lin**, " A Non-Convex Optimization Framework for Large-Scale Low-Rank Matrix Factorization," *Machine Learning with Applications*, Elsevier, vol. 10, p.100440. 2022.

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[J21] W. Wang and **B. Lin**, "Optimizing 3D U-Net-based Brain Tumor Segmentation with Integer-arithmetic Deep Learning Accelerators," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 18, no. 2, pp. 25:1-25:16, 2022.

[J22] D. Lee, **B. Lin** and C.-K. Cheng, "SMT-Based Contention-Free Task Mapping and Scheduling on 2D/3D SMART NoC with Mixed Dimension-Order Routing," *ACM Transactions on Architecture and Code Optimization*, vol. 19, no. 1, pp. 5:1-5:21, 2022.

[J23] D. Dang, **B. Lin** and D. Sahoo, "LiteCON: An All-photonic Neuromorphic Accelerator for Energy-efficient Deep Learning," *ACM Transactions on Architecture and Code Optimization*, vol. 19, no. 3, pp. 43:1-43:22, 2022.

[J24] C.-K. Cheng, C.-T. Ho, C. Holtz, D. Lee and **B. Lin**, "Machine Learning Prediction for Design and System Technology Co-Optimization Sensitivity Analysis," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 8, pp. 1059-1072, 2022.

[J25] C.-K. Cheng, C.-T. Ho, D. Lee, and **B. Lin**, "Multi-row complementary-FET (CFET) standard cell synthesis framework using satisfiability modulo theories (SMTs)," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 1, pp. 43-51, 2021.

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[J37] P. Yin, S. Yang, J. Xu, J. G. Dai and **B. Lin**, "Efficient Traffic Load-Balancing via Incremental Expansion of Routing Choices," *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*, vol. 4, no. 1, pp. 1:1-1:35, 2019.

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[J48] H. Wang and **B. Lin**, "Per-Flow Queue Management with Succinct Priority Indexing Structures for High Speed Packet Scheduling," *IEEE Transactions on Parallel and Distributed Systems*, vol. 24, no. 7, pp. 1380-1389, 2013.

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