# Philip Brisk

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Riverside, CA 92521
[redacted]


## Education

- **Ph.D.** Computer Science, University of California, Los Angeles, 2006
  Advisor: Majid Sarrafzadeh
  Thesis: "Advances in Static Single Assignment Form and Register Allocation"
- **M.S.** Computer Science, University of California, Los Angeles, 2003
  Advisor: Majid Sarrafzadeh
  Thesis: "An Algorithm for the Generation of Parallel Instructions for Reconfigurable Processors"
- **B.S.** Computer Science, University of California, Los Angeles, 2002
- **A.A.** Santa Monica College, General Science, 1999

## Appointments

- **2019-present** Professor, Department of Computer Science and Engineering (Cooperating Faculty, Department of Electrical Engineering), University of California, Riverside
- **2019** Visiting Faculty, Lawrence Berkeley National Laboratory, Berkeley, CA
- **2016-2017** Visiting Professor (Professeur Invité; Sabbatical), École Polytechnique Fédérale de Lausanne (EPFL)
- **2015-2019** Associate Professor, Department of Computer Science and Engineering (Cooperating Faculty, Department of Electrical Engineering), University of California, Riverside
- **2009-2015** Assistant Professor, Department of Computer Science and Engineering (Cooperating Faculty, Department of Electrical Engineering), University of California, Riverside
- **2006-2009** Postdoctoral Scholar, Processor Architecture Laboratory, École Polytechnique Fédérale de Lausanne (EPFL); Supervisor: Paolo Ienne
- **2006** Research Intern, Processor Architecture Laboratory, École Polytechnique Fédérale de Lausanne (EPFL); Supervisor: Paolo Ienne
- **2005** Technology Transfer Internship, Office of Intellectual Property Administration, University of California, Los Angeles
- **2002-2006** Research/Teaching Assistant, Embedded and Reconfigurable System Laboratory, Department of Computer Science, University of California, Los Angeles
- **2002** Laboratory Assistant, Automated Reasoning Group, Department of Computer Science, University of California, Los Angeles

## Research Interests

- Programmable Microfluidics, Field Programmable Gate Arrays, Application-specific Processors
- Design Automation Methodologies for Semiconductor Hardware
- Time-series Data Mining and Applications

## UCR Service

### *Campus*

1. Chancellor's Advisory Committee on the Status of Women, 2020-present
2. Selection Committee, 2021-2022 UCR Women's Initiative
3. AVC/CIO Search Committee, 2020, 2021-present
4. Graduate Careers Working Group, 2020-present
5. Undergraduate Research Symposium Advisory Committee, 2021
6. Provost/EVC Search Committee, 2020
7. Chancellor's Research Fellowship Evaluation Committee, 2019, 2020
8. Reviewer, Faculty Led Education Abroad Program, 2018, 2019
9. Provost's Faculty Leadership Program, 2017-2018
10. Graduate Research Mentoring Program, 2014-2015, 2017-present

### *UCR Academic Senate Division*

1. Executive Council (as BCOE Chair of the Faculty), 2019-present
2. Member, Committee on Diversity, Equity, and Inclusion, 2018-present
3. Chair, Committee on Courses, 2015-2016
4. Member, Committee on Courses, 2013-2015

### *Bourns College of Engineering*

1. BCOE Faculty Equity Advisor, 2019-present
2. Chair of the Faculty, 2019-present
3. Strategic Planning Committee, 2020
4. BCOE Executive Committee, Computer Science Dept. Representative, 2017-2019
5. BCOE Scholarship Committee, 2015

### *Computer Science Department*

1. Colloquium Committee, 2012-2014.

### *Computer Engineering Program*

1. ABET Assessment Coordinator, 2014-2016, 2017-2019
2. Undergraduate Faculty Advisor, 2014-2016

## Awards and Honors

- **ACM SIGPLAN Research Highlight**, OOPSLA 2018
- **Distinguished Paper Award**, OOPSLA 2018
- **Best Paper Award Nominee**, CASES 2017
- **Best Paper Award Nominee**, DAC 2017
- **NSF CAREER Award**, 2014
- **Best Paper Award Nominee**, HiPEAC 2010
- **Michael Servit Best Paper Award**, FPL 2009
- **HiPEAC Paper Award**, DAC 2009
- **HiPEAC Paper Award**, FCCM 2009
- **Best Paper Award**, CASES 2007

- **Best Paper Award Nominee**, DAC 2007

## Software Releases

- UC Riverside Digital Microfluidic Biochip (DMFB) Static Synthesis Simulator
  http://microfluidics.cs.ucr.edu/

## Grants and Fundraising

*National Science Foundation (NSF)*

- #2019632
  FMitF: Track I: Correct-by-Construction Synthesis of Microfluidic Chips
  Dates: 9/30/2020 – 9/29/2024
  Role: Co-PI
  PI: Manu Sridharan, UC Riverside Department of Computer Science and Engineering
  Co-PI: William Grover, UC Riverside, Department of Bioengineering
  Total Amount: $749,147

- #1910878
  FET: Small: Stochastic synthesis of peptides and small molecules
  Dates: 10/1/2019 – 9/30/2022
  Role: Co-PI
  PI: Mohsen Lesani, UC Riverside Department of Computer Science and Engineering
  Co-PI: William Grover, UC Riverside, Department of Bioengineering
  Total Amount: $500,000

- #1763795
  SHF: Medium: Collaborative Research: Predictive Modeling for Next-generation Heterogeneous System Design
  Dates: 9/1/2018 – 8/31/2021
  Role: Co-PI
  PI: Andreas Gerstlauer, University of Text at Austin, Department of Electrical and Computer Engineering
  Co-PI: Lizy K. John, University of Texas at Austin, Department of Electrical and Computer Engineering
  Total Amount: $1,001,941
  UCR Portion: $322,530

- #1740052
  CPS: TTP Option: Medium: Collaborative Research: Low-Cost, High-Throughput, Cyber-Physical Synthesis of Encrypted DNA
  Dates: 10/1/2017 – 9/30/2021
  Role: PI
  Co-PIs: William Grover, UC Riverside, Department of Bioengineering
  Victor Rodgers, UC Riverside, Department of Bioengineering
  Mohammed Al Faruque, UC Irvine, Department of Electrical Engr. and Comp. Sci.
  Subcontract: Richard Morris, CEO, PharmaSeq, Inc.
  Total Amount: $1,323,999
  UCR Portion: $1,039,063 (includes a $300,528 Subcontract to PharmaSeq, Inc.)

- #1640757
  PFI:AIR - TT: Prototyping Microfluidic Very Large Scale Integration Design Automation Tools
  Dates: 9/1/2016 – 2/28/2018
  Role: PI
  Co-PI: William Grover, UC Riverside, Department of Bioengineering

Amount: $199,999, plus
- + $12,000: REU Supplements

- #1560596
  I-Corps: Quick Liquid Layout: Commercialization of Microfluidic Very Large Scale Integration Design Automation Tools
  Dates: 10/1/2015 – 4/30/2017
  Role: PI
  Entrepreneurial Lead: Jeffrey McDaniel, UC Riverside (Ph.D. Candidate, at the time)
  Mentor: Gunnar Hurtig, UC Riverside School of Business Administration
  Co-PI: William Grover, UC Riverside, Department of Bioengineering
  Amount: $50,000

- #1545097
  CPS: Synergy: Collaborative Research: Cyber-physical Digital Microfluidics based on Active Matrix Electrowetting Technology: Software-programmable High-density Pixel Arrays
  Dates: 9/15/2015 – 8/31/2020
  Role: PI
  Co-PI: Philip Rack, University of Tennessee, Knoxville, Department of Tennessee Knoxville, Department of Materials Science and Engineering, and Oak Ridge National Laboratory
  Total Amount: $652,766
  UCR Portion: $352,767, plus
  - $16,000: REU Supplements

- #1536026
  AitF: EXPL: Algorithmic Fluid Concentration Management for Programmable Microfluidics
  Dates: 10/1/2015 – 9/30/2020
  Role: PI
  Co-PIs: Marek Chrobak, UC Riverside, Department of Computer Science and Engineering
  William Grover, UC Riverside, Department of Bioengineering
  Amount: $361,801, plus
  - $16,000: REU Supplements

- #1528181
  CCF: SHF: Small: Collaborative Research: Domain-specific Reconfigurable Processor for Time-Series Data Mining and Monitoring
  Dates: 9/1/2015 – 8/31/2020
  Role: PI
  Co-PI: Abdullah Mueen, University of New Mexico, Department of Computer Science
  Total Amount: $507,152, plus
  - $97,956: NSF-NCS (Neural and Cognitive Systems) Supplement
  UCR Portion: $262,206, plus
  - $49,041: NSF-NCS (Neural and Cognitive Systems) Supplement

- #1423414
  CCF: Design Automation for Paper Microfluidics
  Dates: 10/1/2014 – 9/30/2019
  Role: PI
  Co-PI: William Grover, UC Riverside, Department of Bioengineering)
  Amount: $300,000, plus
  - $48,000: REU Supplements

- #1351115
  CAREER: Design Automation for Microfluidic Large Scale Integration Laboratories-on-a-Chip,
  Dates: 3/1/2014 – 2/28/2020
  Role: PI
  Co-PIs: None
  Amount: $493,645, plus:
    - $13,199: Supplement, Research Opportunities in Europe for NSF CAREER Awardees

- #1059827
  Workshop: Support for the Sixteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2011.
  Dates: 1/15/2011 – 6/30/2011
  Role: PI
  Co-PI: Rajiv Gupta, UC Riverside, Department of Computer Science and Engineering
  Amount: $15,000

- #1035603
  CPS: Small: System Support for Generally Programmable Digital Microfluidic Biochip Devices
  Dates: 9/15/2010 – 8/31/2015
  Role: PI
  Co-PIs: None
  Amount: $539,999, plus:
    - + $32,000: REU Supplements

*Bill & Melinda Gates Foundation*

- #OPP1191214 (Phase I)
  The medical record is in the sample: "Salting" specimens with microtransponder chips to permanently link samples with data
  Dates: 5/01/2018 – 10/31/2019
  Role: Co-PI
  PI: William Grover (UC Riverside, Department of Bioengineering)
  Amount: $100,000

*UC/UCR*

- UCR Office of the Provost/EVC, A Special Session on Computational Microfluidics at the 2018 UC System-wide Bioengineering Symposium, 1/24/2018 – 1/23/2019. ($3,000)
- UC Education Abroad Program, Integrating UCEAP-Supported Study Abroad into UCR Computer Science, 12/14/2017 – 1/30/2019. ($5,000)
- UCR Office of Undergraduate Education Research/Creative Activity Mini-Grant, Use of Biocompatible Piezoelectric Discs in Microbioreactors on PCB; awarded to Mathew Schaffrath, with me as Faculty Mentor. 7/21/2017 - 6/30/2018 ($742)
- UCR 2016-2017 Proof of Concept Funding for Technology Commercialization (PoC) Award Program, A Planar Placement and Routing Algorithm for Flow-Based Microfluidics ($29,090).
- UC Riverside Regents' Faculty Fellowship, How to Program 1000 Cores: Software Development for Massively Parallel Processor Arrays, 2014-2016 ($4,000)
- UC Riverside Regents' Faculty Fellowship, Compiling Chemical Reactions onto Digital Microfluidic Laboratories-on-Chip, 2010-2013. ($4,500)

- UC Riverside Omnibus Academic Senate Research Funds, 2013-2014. ($1,125)
- UC Riverside Omnibus Academic Senate Research Funds, 2010-2013. ($1,260)

### *Xilinx Corporation*

- Xilinx Corporation, Equipment: 2 EK-V6-ML605-G (Virtex 6) development boards, 2011.
- Xilinx Corporation, Equipment: 2 DK-V7-VC709-G (Virtex 7) development boards; Software: Vivado Design Suite, Systems Ed. / ISE Design Suite, Systems Ed. / Partial Reconfiguration Feature for ISE Software, 2013.

### *Intel Corporation*

- Intel Corporation 2019: $15,106
  - 2x Intel® Optane SSD DC D4800X Series (1.5TB, 2.5in PCIe 2x2, 3D XPoint) Dual Port
  - 2x Intel® SSD D3-S4510 Series (1.92TB, 2.5in SATA 6Gb/s, 3D2, TLC) Dell PE Single Pack
  - 2x Intel® SSD DC D4512 Series (1.9TB, 2.5in PCIe 3.1 2x2, 3D2, TLC) Generic Single Pack
  - 2x Intel® SSD D3-S4610 Series (960GB, 2.5in SATA 6Gb/s, 3D2, TLC) HP ISS Single Pack
- Intel Corporation, Hardware Accelerator Research Program, Remote access to a HARP2 Xeon+FPGA (Broadwell + Arria10) cluster. 2016.
- Intel Corporation, Embedded Curriculum Development 2015: $15,000.
- Intel Corporation, Embedded Curriculum Development, Equipment: 10 Intel Galileo Development Boards 2014. ($10,000)
- Intel Corporation, Embedded Curriculum Development, Equipment: 15 Terasic DE2i-150 FPGA Development Kits 2013. ($20,000)
- Intel Corporation, Hardware/Software Co-Design for Intel Atom Tunnel Creek / Altera Cyclone IV Development Boards, 2012. ($20,000)
- Intel Corporation, Intel Embedded Curriculum Support for Undergraduate Embedded Systems Education at UC Riverside, 2011. ($30,000). Co-PI: Laxmi Bhuyan (UC Riverside)

### *Other/Uncategorized*

- Bavaria California Technology Center (BaCaTeC), Techniques to Enhance the Arithmetic Capabilities and Performance of Reconfigurable Computing Platforms, 2012-2013. (€6,000). PI: Frank Hannig (University of Erlangen-Nuremberg)
- Oak Ridge National Laboratory (ORNL), Center for Nanophase Materials Sciences. User Nanoscience Research Program. 2016-2017. Co-PI: Philip Rack (University of Tennessee and Oak Ridge National Laboratory); Technical Contact: Scott Retterer (Oak Ridge National Laboratory)

## Publications

### *Book Chapters*

1. Tammara Massey, Foad Dabiri, Roozbeh Jafari, Hyduke Noshadi, Philip Brisk, and Majid Sarrafzadeh. “Reconfigurable medical embedded systems,” in A. Lazakidou and K. Siassiakos, eds., Handbook of Research on Distributed Medical Informatics and E-Health, IGI Global, 2008.
2. Philip Brisk and Majid Sarrafzadeh. “Datapath synthesis,” in: Paolo Ienne and Rainer Leupers, eds., Customizable and Configurable Embedded Processors: Design Technologies and Applications, Elsevier, 2006.

*Journals*

1. Joshua Potter, William H. Grover, Philip Brisk. "Dynamic Radial Placement and Routing in Paper Microfluidics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. Accepted for publication; to appear.
2. Brian Crites, Cody Falzone, Tristan Lopez, Karen Kong, and Philip Brisk. "Reducing Microfluidic Very Large Scale Integration (mVLSI) Chip Area by Seam Carving," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. Accepted for publication; to appear.
3. Jason Ott, Tyson Loveless, Chris Curtis, Mohsen Lesani, and Philip Brisk. "BioScript: Programming Safe Chemistry on Laboratories-on-a-Chip," *Communications of the ACM. Research Highlights Article.* Accepted for publication; to appear.
4. Jason Ott, Daniel Tan, Tyson Loveless, William Grover, and Philip Brisk. "ChemStor: Using formal methods to guarantee safe storage and disposal of chemicals," *Journal of Chemical Information and Modeling (JCIM)*: 60(7): 3416-3422, 2020.
5. Brian Crites, Karen Kong, and Philip Brisk. "Directed Placement for mVLSI Devices," *ACM Journal on Emerging Technologies in Computing (JETC)* 16(2): article #14, December, 2019.
6. Junchao Wang, Naiyin Zhang, Jin Chen, Victor G. J. Rodgers, Philip Brisk, and William H. Grover. "Finding the optimal design of a microfluidic mixer," *Lab-on-a-Chip* 19(21): 3618-3627, October, 2019.
7. Walker L. Boldman, Cheng Zhang, Thomas Z. Ward, Dayrl P. Briggs, Bernadeta R. Srijanto, Philip Brisk, and Philip D. Rack. "Programmable electrofluidics for ionic liquid based neuromorphic platform," *Micromachines* 10(7):478-486, July, 2019.
8. Kenneth O'Neal, Philip Brisk, Emily Shriver, and Michael Kishinevsky. "Hardware-assisted cross-generation prediction of GPUs under design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 38(6):1133-1146, June, 2019.
9. Joshua Potter, Philip Brisk, and William H. Grover. "Using printer ink to control the behavior of paper microfluidics," *Lab-on-a-Chip* 19(11):2000-2008, May, 2019.
10. Brittney A. McKenzie, Jessica Robles-Najar, Eric Duong, Philip Brisk, and William H. Grover. "Chronoprints: identifying samples by visualizing how they change over space and time," *ACS Central Science* 5(4): 589-598, March 2019.
11. Alireza Abdoli and Philip Brisk. "Stationary-mixing field-programmable pin-constrained digital microfluidic biochip," *Microelectronics Journal*, 77:34-48, July 2018.
12. Wajid Hassan Minhass, Jeffrey McDaniel, Michael Raagaard, Philip Brisk, Paul Pop, and Jan Madsen. "Scheduling and fluid routing for flow-based microfluidic laboratories-on-a-chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 37(3):615-628, March, 2018.
13. Kenneth O'Neal, Daniel Grissom, and Philip Brisk. "Resource-constrained scheduling for digital microfluidic biochips," *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, 14(1): article #7, March, 2018.
14. Yan Zhu, Zachary Zimmerman, Nader Shakibay Senobari, Chin-Chia Michael Yeh, Gareth Funning, Abdullah Mueen, Philip Brisk and Eamonn Keogh. "Exploiting a novel algorithm and GPUs to break the ten quadrillion pairwise comparison barrier for time series motifs and joins," *Knowledge and Information Systems (KAIS)*, 54(1): 203-236, January, 2018.
15. Junchao Wang, Victor G. J. Rodgers, Philip Brisk, and William H. Grover. "Instantaneous simulation of fluids and particles in complex microfluidic devices. *PLoS ONE*, 12(12): e0189429, December, 2017.

16. Brian Crites, Karen Kong, and Philip Brisk. “Diagonal component expansion for flow-layer placement of flow-based microfluidic biochips,” *ACM Transactions on Embedded Computing Systems (TECS)*, 16(5s): article #126, October, 2017.
17. Lana Josipovic, Philip Brisk, and Paolo Ienne. “An out-of-order load-store queue for spatial computing,” *ACM Transactions on Embedded Computing Systems (TECS)*, 16(5s): article #125, October, 2017.
18. Kenneth O'Neal, Philip Brisk, Zack Waters, Ahmed Abousamra and Emily Shriver. “GPU performance estimation using software rasterization and machine learning,” *ACM Transactions on Embedded Computing Systems (TECS)*, 16(5s): article #148, October, 2017.
19. Junchao Wang, Victor G. J. Rodgers, Philip Brisk, and William H. Grover. “MOPSA: a microfluidics-optimized particle simulation algorithm,” *Biomicrofluidics (BMF)*, 11(3): 034121, May, 2017.
20. Skyler Windh, Calvin Phung, Daniel Grissom, Paul Pop, and Philip Brisk. “Performance improvements and congestion reduction for routing-based synthesis for digital microfluidic biochips,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 36(1):41-54, January, 2017.
21. Jeffrey McDaniel, Zachary Zimmerman, Daniel Grissom, and Philip Brisk. “PCB escape routing and layer minimization for digital microfluidic biochips,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 36(1):69-82, January, 2017.
22. Junchao Wang, Philip Brisk, and William Grover. “Random design of microfluidics,” *Lab-on-a-Chip*, 16(21):4212-4219, October, 2016.
23. Jeffrey McDaniel, Brian Crites, William Grover, and Philip Brisk. “Flow layer physical design for microfluidic chips based on monolithic membrane valves,” *IEEE Design & Test*, 32(6):51-59, December, 2015.
24. Yehdhih Ould Mohammed Moctar, Guy G. F. Lemieux, and Philip Brisk. “Fast and memory-efficient routing algorithms for field programmable gate arrays with sparse intra-cluster routing crossbars,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 34(12):1928-1941, December, 2015.
25. Christopher Curtis and Philip Brisk. “Simulation of feedback-driven PCR assays on a 2D electrowetting array using a domain-specific high-level biological programming language,” *Microelectronics Journal*, 148(1):110-116, December, 2015.
26. Daniel Grissom, Christopher Curtis, Skyler Windh, Calvin Phung, Naveen Kumar, Zachary Zimmerman, Kenneth O’Neal, Jeffrey McDaniel, Nick Liao, and Philip Brisk. “An open-source compiler and PCB synthesis tool for digital microfluidic biochips,” *Integration: The VLSI Journal*, 51:169-193, September, 2015.
27. Ali Galip Bayrak, Francesco Regazzoni, David Novo Bruna, Philip Brisk, François-Xavier Standaert, and Paolo Ienne. “Automatic application of power analysis countermeasures,” *IEEE Transactions on Computers (TC)*, 64(2):329-341, February, 2015.
28. Bailey Miller, Frank Vahid, Tony Givargis, and Philip Brisk. “Graph-based approaches to placement of processing element networks on FPGAs for physical model simulation,” *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 7(4): article #10, December, 2014.
29. Daniel Grissom, Jeffrey McDaniel, and Philip Brisk. “A Low-cost field-programmable pin-constrained digital microfluidic biochip,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 33(11): 1657-1670, November, 2014.
30. Theo Kluter, Samuel Burri, Philip Brisk, Edoardo Charbon, and Paolo Ienne. “Virtual ways: low-cost coherence for instruction set extensions with architecturally visible storage,” *ACM Transactions on Architecture and Code Optimization (TACO)*, 11(2), article #15, June, 2014.

31. Daniel Grissom, Christopher Curtis, and Philip Brisk. “Interpreting assays with control flow on digital microfluidic biochips,” *ACM Journal on Emerging Technologies in Computing (JETC)*, 10(3): article #24, April, 2014.

32. Daniel Grissom, and Philip Brisk. “Fast online synthesis of digital microfluidic biochips,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 33(3):356-359, February, 2014.

33. Ismail Emre Araci, and Philip Brisk. “Recent developments in microfluidic large scale integration,” *Current Opinion in Biotechnology*, 25:60-68, February, 2014.

34. Theo Kluter, Philip Brisk, Edoardo Charbon, and Paolo Ienne. “Way stealing: a unified data cache and architecturally visible storage for instruction set extensions,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* 22(1): 62-75, January, 2014.

35. Mirjana Stojilovic, David Novo, Lazar Saranovac, Philip Brisk, and Paolo Ienne. “Selective flexibility: creating domain-specific reconfigurable arrays,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Sytems (TCAD)*, 32(5):681-694, May, 2013.

36. Benoit Boissinot, Philip Brisk, Alain Darte, and Fabrice Rastello. “SSI revisited,” *ACM Transactions on Embedded Computing Systems (TECS)*, Special Issue on Software and Compilers for Embedded Systems, 11S(1): article #21 (23 pages), June, 2012.

37. Hadi Parandeh-Afshar, Arkosnato Neogy, Philip Brisk, and Paolo Ienne. “Compressor tree synthesis on commercial high-performance FPGAs, *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 4(4): article #39 (19 pages), December, 2011.

38. Philip Brisk, Ajay K. Verma, and Paolo Ienne. “An optimal linear-time algorithm for interprocedural register allocation in high level synthesis using SSA Form,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 29(7):1096-1109, July, 2010.

39. Hadi Parandeh-Afshar, Ajay K. Verma, Philip Brisk, and Paolo Ienne. “Improving FPGA performance for carry-save arithmetic,” *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, 18(4): 578-590, April, 2010.

40. Ajay K. Verma, Philip Brisk, and Paolo Ienne. “Fast, nearly optimal ISE identification with I/O serialization through maximal clique enumeration” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 29(3):341-354, March, 2010.

41. Ani Nahapetian, Philip Brisk, Soheil Ghiasi, and Majid Sarrafzadeh. “An approximation algorithm for scheduling on heterogeneous reconfigurable resources,” *ACM Transactions on Embedded Computing Systems (TECS)*, 9(1): article #5 (20 pages), October, 2009.

42. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. “An FPGA logic cell configurable as a 6:2 or 7:2 compressor,” *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 2(3): article #19 (42 pages), September, 2009.

43. Alessandro Cevrero, Panagiotis Athanasopoulos, H. Parandeh-Afshar, A. K. Verma, P. Brisk, Hosein Seyed Attarzadeh, Niaki, Chrysostomos Nicopoulos, Frank K. Gurkaynak, Yusuf Leblebici, and Paolo Ienne. “Field programmable compressor trees: acceleration of multiinput addition on FPGAs,” *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 2(2): article #13 (36 pages), June, 2009.

44. Ajay K. Verma, Philip Brisk, and Paolo Ienne. “Dataflow transformations to maximize the use of carry-save representation in arithmetic circuits,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 27(10):1761-1774, October, 2008.

45. Philip Brisk, Ajay K. Verma, and Paolo Ienne. “Optimistic chordal coloring: a coalescing heuristic for SSA Form programs,” *Springer Journal on Design Automation for Embedded Systems (DAES)*, ESWeek 2007 Special Issue, 2008.

46. Philip Brisk, Foad Dabiri, Roozbeh Jafari, and Majid Sarrafzadeh. “Optimal register sharing for high-level synthesis of SSA form programs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 25(5):772-779, May, 2006.

*Conferences*

1. Amin Kalantar, Zachary Zimmerman, and Philip Brisk, "FA-LAMP: FPGA-Accelerated Learned Approximate Matrix Profile for Time Series Similarity Prediction," *International Symposium on Field-programmable Custom Computing Machines (FCCM)*, May, 2021. Accepted for publication; to appear.
2. Tyson Loveless, Jason Ott, and Philip Brisk. "Time- and Resource-constrained Scheduling for Digital Microfluidic Biochips," *International Conference on Cyber-Physical Systems (ICCPS)*, May, 2021. Accepted for publication; to appear.
3. Hugo Brunie, Costin Iancu, Khaled Z. Ibrahim, Philip Brisk, and Brandon Cook. "Tuning floating-point precision using dynamic program information and temporal locality." *The International Conference for High-Performance Computing, Networking, Storage, and Analysis (Supercomputing/SC)*, November, 2020, pp. 50:1-50:14.
4. Tyson Loveless, Jason Ott, and Philip Brisk. "A Performance-Optimizing Compiler for Cyber-Physical Digital Microfluidic Biochips," *International Conference on Code Generation and Optimization (CGO)*, February, 2020, pp. 171-184.
5. Frederic Gessler, Philip Brisk, and Mirjana Stojilovic. "A Shared-memory Parallel Implementation of the RePlAce Global Cell Placer," *VLSI Design (VLSID)*, January, 2020.
6. Sina Boroumand and Philip Brisk. "Approximate Adder Tree Synthesis for FPGAs," *International Conference on Reconfigurable Computing and FPGAs (ReConFig)* December, 2019, pp. 1-8 **(Best Paper Award)**
7. Zachary Zimmerman, Kaveh Kamgar, Nader Shakibay Senobari, Yan Zhu, Brian Crites, Gareth Funning, Philip Brisk, and Eamonn Keogh. "Matrix Profile XIV: Scaling Time Series Motif Discovery with GPUs to Break a Quintillion Pairwise Comparisons a Day and Beyond" ACM Symposium on Cloud Computing (SoCC), November, 2019, pp. 74-86.
8. Zachary Zimmerman, Nader Shakibay Senobari, Gareth Funning, Evangelos Papalexakis, Samet Oymak, Philip Brisk, and Eamonn Keogh. "Matrix Profile XVIII: Time Series Mining in the Face of Fast Moving Streams using a Learned Approximate Matrix Profile," *IEEE International Conference on Data Mining (ICDM)*, November, 2019, pp. 936-945.
9. Radhakrishna Sanka, Brian Crites, Jeffrey McDaniel, Philip Brisk, and Douglas Densmore. "Specification, Integration and Benchmarking of Continuous Flow Microfluidic Devices," *International Conference on Computer-Aided Design (ICCAD)*, November, 2019, pp. 1-8.
10. Sina Faezi, Sujit Rokka Chhetri, Arnav Vaibhav Malawade, John Charles Chaput, William H. Grover, Philip Brisk, and Mohammad Abdullah Al Faruque. "Oligo-Snoop: a non-invasive side channel attack against DNA synthesis machines," *Network and Distributed System Security Symposium (NDSS)*, February, 2019.
11. Jason Ott, Tyson Loveless, Christopher Curtis, Mohsen Lesani, and Philip Brisk. "BioScript: programming safe chemistry of laboratories-on-a-chip," *Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA)*, Boston, MA, USA, November, 2018. Published in Proceedings of the ACM on Programming Languages (PACMPL) 128:1-128:31, November, 2018. **(Distinguished Paper Award)**
12. Kenneth O'Neal, Mitch Liu, Hans Tang, Amin Kalantar, Kennen DeRenard and Philip Brisk. "HLSPredict: cross platform performance prediction for FPGA high-level synthesis," *International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, USA, November, 2018, pp. 104:1 – 104:8.
13. Brian Crites, Radhakrishna Sanka, Joshua Lippai, Jeffrey McDaniel, Philip Brisk, and Douglas Densmore. "ParchMint: A Microfluidics Benchmark Suite," *IEEE International Symposium on Workload Characterization (IISWC)*, Raleigh, North Carolina, September-October 2018 (Short paper; poster presentation).

14. Yehdhih Ould Mohammed Moctar, Mirjana Stojilovic, and Philip Brisk. “Deterministic parallel routing for FPGAs based on Galois parallel execution model,” *International Symposium on Field Programmable Logic and Applications (FPL)*, Dublin, Ireland, August 2018 (Short paper; poster presentation).
15. Junchao Wang, Lingxuan Fu, Liyang Yu, Xiwei Huang, Philip Brisk, and William H. Grover. “Accelerating simulation of particle trajectories in microfluidic devices by constructing a cloud database,” *International Symposium on VLSI (ISVLSI)*, Hong Kong SAR, July 2018, pp. 666-671. (Invited paper).
16. Kenneth O’Neal and Philip Brisk. “Predictive modeling for CPU, GPU, and FPGA performance and power consumption: a survey,” *International Symposium on VLSI (ISVLSI)*, Hong Kong SAR, July 2018, pp. 763-768 (Invited paper).
17. Sina Boroumand, Hadi P. Afshar, and Philip Brisk. “Approximate quaternary addition with the fast carry chains of FPGAs,” *Design Automation and Test in Europe (DATE)*, March, 2018, pp. 577-580. (Short paper; interactive presentation).
18. Christopher Curtis, Daniel Grissom, and Philip Brisk. “A compiler for cyber-physical digital microfluidic biochips,” *International Symposium on Code Generation and Optimization (CGO)*, February, 2018, pp. 365-377.
19. Sina Boroumand, Hadi P. Afshar, Philip Brisk, and Siamak Mohammadi. “Exploration of approximate multipliers design space using carry propagation free compressors,” *Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2018, pp. 611-616.
20. Lana Josipovic, Philip Brisk, and Paolo Ienne. “From C to Elastic Circuits,” *51st Asilomar Conference on Signals, Systems, and Computers*, October-November, 2017, pp. 121-125.
21. Sina Boroumand, Hadi P. Afshar, Philip Brisk, and Siamak Mohammadi. “CAL: exploring cost, accuracy, and latency in approximate and speculative adder design,” *30th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, October, 2017.
22. Kenneth O'Neal, Philip Brisk, Zack Waters, Ahmed Abousamra and Emily Shriver. “GPU performance estimation using software rasterization and machine learning,” *International Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS)*, October, 2017. Accepted for publication; to appear. (The paper was presented at the conference, but not published in the conference proceedings; instead it was published in an October 2017 Special Issue of ACM TECS).
23. Brian Crites, Karen Kong, and Philip Brisk. “Diagonal component expansion for flow-layer placement of flow-based microfluidic biochips,” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2017. Accepted for publication; to appear. (The paper was presented at the conference, but not published in the conference proceedings; instead it was published in an October 2017 Special Issue of ACM TECS).
24. Lana Josipovic, Philip Brisk, and Paolo Ienne. “An out-of-order load-store queue for spatial computing,” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2017. Accepted for publication; to appear. (The paper was presented at the conference, but not published in the conference proceedings; instead it was published in an October 2017 Special Issue of ACM TECS).
25. Kenneth O’Neal, Philip Brisk, Emily Shriver, and Michael Kishinevsky. “HALWPE hardware-assisted light weight performance estimation for GPUs,” *54th Design Automation Conference (DAC)*, June, 2017. **(Best Paper Award Nominee)**
26. Andrew Becker, Wei Hu, Yu Tai, Philip Brisk, Ryan Kastner, and Paolo Ienne. “Arbitrary precision and complexity tradeoffs for gate-level information flow tracking,” *54th Design Automation Conference (DAC)*, June, 2017.

27. Joshua Potter, William Grover, and Philip Brisk. “Design automation for paper microfluidics with passive flow substrates,” *Great Lakes Symposium on VLSI (GLSVLSI)*, May, 2017, pp. 215-220.

28. Brian Crites, Karen Kong, and Philip Brisk. “Reducing microfluidic very large scale integration (mVLSI) chip area by seam carving,” *Great Lakes Symposium on VLSI (GLSVLSI)*, May, 2017, pp. 459-462.

29. Lana Josipovic, Philip Brisk, and Paolo Ienne. “An out-of-order load-store queue for spatial computing,” *25th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April-May 2017, p. 134 (1 page paper; poster presentation)

30. Jeffrey McDaniel, William Grover, and Philip Brisk. “The case for semi-automated design of Microfluidic Very Large Scale Integration (mVLSI) Chips,” *Design Automation and Test in Europe (DATE)*, March, 2017, pp. 1793-1798. (Special Session: Cyberphysical Microfluidic Biochips: EDA Challenges and Opportunities to Bridge the Gap Between Microfluidics and Microbiology)

31. Yan Zhu, Zachary Zimmerman, Nader Shakibay Senobari, Chin-Chia Michael Yeh, Gareth Funning, Abdullah Mueen, Philip Brisk and Eamonn Keogh. “Matrix profile II: exploiting a novel algorithm and GPUs to break the one hundred million barrier for time series motifs and joins,” *IEEE International Conference on Data Mining (ICDM)*, December, 2016.

32. Jeffrey McDaniel, Brian Crites, Christopher Curtis, and Philip Brisk. “Design automation for flow-based microfluidic biochips,” *37th Annual International conference of the IEEE Engineering in Medicine and Biology Society. Mini-Symposium: Continuous-Flow Biochips: Technology, Testing, and Design for Fault-Tolerance and Reliability*, August, 2015 (1 page).

33. Christopher Jaress, Philip Brisk, and Daniel Grissom. “Rapid online fault recovery for cyber-physical digital microfluidic biochips,” *IEEE VLSI Test Symposium (VTS)*, April, 2015, pp. 1-6.

34. Daniel Grissom, Jeffrey McDaniel, and Philip Brisk. “Performance and cost analysis of NoC-inspired virtual topologies for digital microfluidic biochips,” *IEEE International Symposium on Integrated Circuits (ISIC)*, December, 2014, pp. 352-355. (Special Session: The Coming of Age of Microfluidics: EDA Solutions for Enabling Biochemistry on a Chip)

35. Joseph Tarango, Eamonn Keogh, and Philip Brisk. “Accelerating the Dynamic Time Warping Distance Measure using Logarithmic Arithmetic,” *48th Asilomar Conference on Signals, Systems and Computers*, November, 2014, pp. 404-408.

36. Jeffrey McDaniel, Brendon Parker, and Philip Brisk. “Simulated annealing-based placement for microfluidic large scale integration (mLSI) chips,” *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October, 2014, pp. 213-218.

37. Jeffrey McDaniel, Daniel Grissom, and Philip Brisk. “Multi-terminal PCB escape routing for digital microfluidic biochips using negotiated congestion,” *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October, 2014, pp. 219-224.

38. Daniel Grissom and Philip Brisk. “Software Control of Cyber-physical Laboratories-on-Chip,” *36th Annual International conference of the IEEE Engineering in Medicine and Biology Society. Mini-Symposium: Health Cyber-Physical Systems: Present Status and Future Directions II*, August, 2014.

39. Yehdhih Ould Mohammed Moctar and Philip Brisk. “Parallel FPGA routing based on the operator formulation,” *Design Automation Conference (DAC)*, June 2014.

40. Johnathan Fiske, Daniel Grissom, and Philip Brisk. “Exploring speed and energy tradeoffs in droplet transport for digital microfluidic biochips,” *Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2014, pp. 231-237.

41. Liang Chen, Joseph Tarango, Tulika Mitra, and Philip Brisk. “A just-in-time customizable processor,” *International Conference on Computer-Aided Design (ICCAD)*, November, 2013, pp. 524-531.

42. Jeffrey McDaniel, Christopher Curtis, and Philip Brisk. “Automatic synthesis of microfluidic large scale integration chips from a domain-specific language,” *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, October-November, 2013, pp. 101-104.

43. Joseph Tarango, Eamonn Keogh, and Philip Brisk. “Instruction set extensions for dynamic time warping,” *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, September-October, 2013.

44. Sambit Shukla, Yang Yang, Laxmi N. Bhuyan, and Philip Brisk. “Shared memory heterogeneous computation on PCIe-supported platforms,” *23rd International Conference on Field Programmable Logic and Applications (FPL)*, September, 2013.

45. Daniel Grissom and Philip Brisk. “A field-programmable pin-constrained digital microfluidic biochip,” *50th Design Automation Conference (DAC)*, June 2013, article #46.

46. Ali Galip Bayrak, Nikola Velickovic, Francesco Regazzoni, David Novo, Philip Brisk, and Paolo Ienne. “An EDA-friendly protection scheme against side-channel attacks,” *Design Automation and Test in Europe (DATE)*, March, 2013, pp. 410-415.

47. Jeffrey McDaniel, Auralila Baez, Brian Crites, Aditya Tammewar, and Philip Brisk. “Design and verification tools for continuous fluid flow-based microfluidic devices,” *Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2013, pp. 219-224 (Special Session: Design Automation for Flow-based Microfluidic Biochips: Connecting Biochemistry to Electric Design Automation).

48. Daniel Grissom, Kenneth O’Neal, Benjamin Preciado, Hiral Patel, Robert Doherty, Nick Liao, and Philip Brisk. “A Digital Microfluidic Biochip Synthesis Framework,” *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October, 2012, pp. 177-182.

49. Kenneth O’Neal, Daniel Grissom, and Philip Brisk. “Force-directed List Scheduling for Digital Microfluidic Biochips, *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October, 2012, pp. 7-12.

50. Daniel Grissom and Philip Brisk. “Fast online synthesis for generally programmable digital microfluidic biochips,” *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, October, 2012, pp. 413-422.

51. Yehdhih Ould Mohammed Moctar, Guy G. F. Lemieux, and Philip Brisk. “Routing algorithms for FPGAs with sparse intra-cluster routing crossbars,” *22nd International Conference on Field Programmable Logic and Applications (FPL)*, August, 2012, pp. 91-98.

52. Aanjhan Ranghanathan, Ali Galip Bayrak, Theo Kluter, Edoardo Charbon, Paolo Ienne, and Philip Brisk. “Counting stream registers: an efficient and effective snoop filter architecture,” *International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XII)*, July 2012, pp. 120-127.

53. Daniel Grissom and Philip Brisk. “Path scheduling on digital microfluidic biochips,” *Design Automation Conference (DAC)*, June, 2012, pp. 26-35.

54. Daniel Grissom and Philip Brisk. “A high-performance assay interpreter for digital microfluidic biochips,” *Great Lakes Symposium on VLSI (GLS-VLSI)*, May, 2012, pp. 103-106.

55. Mirjana Stojilovic, David Novo, Lazar Saranovac, Philip Brisk, and Paolo Ienne. “Selective flexibility: breaking the rigidity of datapath merging,” *Design Automation and Test in Europe (DATE)*, March, 2012, pp. 1543-1548.

56. Yehdhih Ould Mohammed Moctar, Nithin George, Hadi Parandeh-Afshar, Paolo Ienne, Guy G. F. Lemieux, and Philip Brisk. “Reducing the cost of floating-point mantissa alignment and normalization in FPGAs,” *20th International Symposium on FPGAs (FPGA)*, February, 2012, pp. 255-264.

57. Philip Brisk. “Architecture and design automation for application-specific processors,” *9th IEEE International Conference on ASIC (ASICON)*, October, 2011, pp. 1179-1182. (Special Session: High-level Synthesis)

58. Quentin Columbet, Benoit Boissinot, Philip Brisk, Sebastian Hack, and Fabrice Rastello. "Graph coloring and treescan register allocation using repairing," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2011, pp. 45-54.

59. Ali Galip Bayrak, Franceso Regazzoni, Philip Brisk, François-Xavier Standaert, and Paolo Ienne. "A first step towards automatic application of power analysis countermeasures," *48th Design Automation Conference (DAC)*, June, 2011, pp. 230-235.

60. Hadi Parandeh-Afshar, Grace Zgheib, Philip Brisk, and Paolo Ienne. "Reducing the pressure on routing resources of FPGAs with generic logic chains," *19th International Symposium on FPGAs (FPGA)*, February, 2011, pp. 237-246.

61. Amit Verma, Ajay K. Verma, Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. "Synthesis of floating-point addition clusters on FPGAs using carry-save arithmetic," *20th International Conference on Field Programmable Logic and Applications (FPL)*, September, 2010, pp. 19-24.

62. Theo Kluter, Samuel Burri, Philip Brisk, Edoardo Charbon, and Paolo Ienne. "Virtual ways: efficient coherence for architecturally visible storage in automatic instruction set extensions," *International Conference on High-Performance Embedded Architecture and Compilers (HiPEAC)*, January, 2010, pp. 126-140. **(Best Paper Award Nominee)**

63. Nagaraju Pothineni, Philip Brisk, Paolo Ienne, Anshul Kumar, and Kolin Paul. "A high-level synthesis flow for custom instruction set extensions for application-specific processors," *15th Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2010, pp. 707-712.

64. Hadi Parandeh-Afshar, Alessandro Cevrero, Panagiotis Athanasopoulos, Philip Brisk, Yusuf Leblebici, and Paolo Ienne. "A flexible DSP block to enhance FPGA arithmetic performance," *International Conference on Field-Programmable Technology (FPT)*, December, 2009, pp. 70-77.

65. Ajay K. Verma, Philip Brisk, and Paolo Ienne. "Iterative layering: optimizing arithmetic circuits by structuring the information flow," *International Conference on Computer-Aided Design (ICCAD)*, November, 2009, pp. 797-804.

66. Panagiotis Athansopoulos, Philip Brisk, Yusuf Leblebici, and Paolo Ienne. "Memory organization and data layout for custom instruction set extensions with architecturally visible storage," *International Conference on Computer-Aided Design (ICCAD)*, November, 2009, pp. 689-696.

67. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. "Exploiting fast carry-chains of FPGAs for designing compressor trees," *19th International Conference on Field-Programmable Logic and Applications (FPL)*, August-September, 2009, pp. 242-249. **(Michal Servit Best Paper Award)**

68. Alessandro Cevrero, Panagiotis Athanasopoulos, Hadi Parandeh-Afshar, Maurizio Skerlj, Philip Brisk, Yusuf Leblebici, and Paolo Ienne. "Using 3D integration technology to realize multi-context FPGAs," *19th International Conference on Field-Programmable Logic and Applications (FPL)*, August-September, 2009, pp. 507-510.

69. Theo Kluter, Philip Brisk, Edoardo Charbon, and Paolo Ienne. "Way stealing: cache-assisted automatic instruction set extensions," *46th Design Automation Conference (DAC), July, 2009, pp. 31-36*. **(HiPEAC Paper Award)**

70. Jose Luis Ayala, David Atienza, and Philip Brisk. "Thermal-aware data flow analysis," *46th Design Automation Conference (DAC)*, Wild and Crazy Idea (WACI) Session, July, 2009, pp. 613-614.

71. Ajay K. Verma, Yi Zhu, Philip Brisk, and Paolo Ienne. "Arithmetic optimization for custom instruction set synthesis," *7th IEEE Symposium on Application-Specific Processors (SASP)*, July, 2009, pp. 54-57.

72. Marcela Zuluaga, Theo Kluter, Philip Brisk, Nigel Topham, and Paolo Ienne. “Introducing control-flow inclusion to support pipelining in custom instruction set extensions,” *7th IEEE Symposium on Application-Specific Processors (SASP)*, July, 2009, pp. 114-121.

73. Ajay K. Verma, Philip Brisk, and Paolo Ienne ”Challenges in automatic optimization of arithmetic circuits,” *19th International Symposium on Computer Arithmetic (ARITH-19)*, June, 2009, pp. 213-218. (Special Session: Automatic Synthesis of Arithmetic Operators)

74. Arun Paidimarri, Alessandro Cevrero, Philip Brisk, and Paolo Ienne. “FPGA implementation of a single-precision floating-point multiply-accumulator with single-cycle accumulation,” *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April, 2009, pp. 267-270. **(HiPEAC Paper Award)**

75. Philip Brisk and Paolo Ienne. “On the complexity of the port assignment problem for binary commutative operators in high-level synthesis,” *International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, April, 2009, pp. 339-342.

76. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. “Scalable and low cost design approach for variable block size motion estimation (VBSME),” *International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, April, 2009, pp. 271-274.

77. Theo Kluter, Philip Brisk, Edoardo Charbon, and Paolo Ienne. “MPSoC design using application-specific architecturally visible communication,” *International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, January, 2009, pp. 183-197.

78. Amit Verma, Ajay K. Verma, Philip Brisk, and Paolo Ienne. “Hybrid LZA: a near optimal implementation of the leading zero anticipator” *Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2009, pp. 203-209.

79. Jani Boutellier, Philip Brisk, and Paolo Ienne. “Insights to variable block size motion estimation by design space exploration,” *Conference on Design and Architecture for Signal and Image Processing (DASIP)*, November, 2008, pp. 307-313.

80. Theo Kluter, Philip Brisk, Paolo Ienne, and Edoardo Charbon “Speculative DMA for architecturally visible storage in instruction set extensions,” *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, October, 2008, pp. 243-248.

81. Hosein Seyed Attarzadeh Niaki, Alessandro Cevrero, Philip Brisk, Chrysostomos Nicopoulos, Frank K. Gurkaynak, Yusuf Leblebici, and Paolo Ienne “Design space exploration for field programmable compressor trees,” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2008, pp. 207-216.

82. Ajay K. Verma, Philip Brisk, and Paolo Ienne “Variable latency speculative adder: a new paradigm for arithmetic circuit design,” *Design Automation and Test in Europe (DATE)*, March, 2008, pp. 1250-1255.

83. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne “Improving synthesis of compressor trees on FPGAs via integer linear programming,” *Design Automation and Test in Europe (DATE)*, March, 2008, pp. 1256-1261.

84. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. “A novel FPGA logic bock for improved arithmetic performance,” *16th International Symposium on FPGAs (FPGA)*, February, 2008, pp. 171-180.

85. Alessandro Cevrero, Panagiotis Athanasopoulos, Hadi Parandeh-Afshar, Ajay K. Verma, Philip Brisk, Frank K. Gurkaynak, Yusuf Leblebici, and Paolo Ienne. “Architectural improvements for field programmable counter arrays: enabling efficient synthesis of fast compressor trees on FPGAs,” *16th International Symposium on FPGAs (FPGA)*, February, 2008, pp. 181-190.

86. Ajay K. Verma, Philip Brisk, and Paolo Ienne. “Fast quasi-optimal and pipelined instruction set extensions,” *13th Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2008, pp. 334-339.

87. Hadi Parandeh-Afshar, Philip Brisk, and Paolo Ienne. "Efficient synthesis of compressor trees on FPGAs," *13th Asia and South Pacific Design Automation Conference (ASPDAC)*, January, 2008, pp. 138-143.

88. Philip Brisk, Ajay K. Verma, and Paolo Ienne. "Optimal polynomial-time interprocedural register allocation for high-level synthesis and ASIP design," *International Conference on Computer-Aided Design (ICCAD)*, November, 2007, pp. 172-179.

89. Philip Brisk, Ajay K. Verma, and Paolo Ienne. "An optimistic and conservative register heuristic for chordal graphs," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2007, pp. 209-217.

90. Ajay K. Verma, Philip Brisk, and Paolo Ienne. "Rethinking custom ISE identification: a new processor-agnostic method," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2007, pp. 125-134. **(Best Paper Award)**

91. Tammara Masssey, Philip Brisk, Foad Dabiri, and Majid Sarrafzadeh. "Delay aware reconfigurable security for embedded systems," *International Conference on Body Area Networks (Bodynets)*, June, 2007, article #12 (5 pages).

92. Ajay K. Verma, Philip Brisk, and Paolo Ienne. "Progressive decomposition: a heuristic to structure arithmetic circuits," *44th Design Automation Conference (DAC)*, June, 2007, pp. 404-409 **(Best Paper Nominee)**

93. Philip Brisk, Ajay K. Verma, Paolo Ienne, and Hadi Parandeh-Afshar. "Enhancing FPGA performance for arithmetic circuits," *44th Design Automation Conference (DAC)*, June, 2007, pp. 334-337.

94. Ryan Kastner, Wenrui Gong, Xin Hau, Forrest Brewer, Adam Kaplan, Philip Brisk, and Majid Sarrafzadeh. "Layout driven data communication optimization for high-level synthesis," *Design Automation and Test in Europe (DATE)*, March, 2006, pp. 1185-1190.

95. Philip Brisk, Jamie Macbeth, Ani Nahapetian, and Majid Sarrafzadeh. "A dictionary construction technique for code compression systems with echo instructions," *ACM/ SIGPLAN Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, June, 2005, pp. 105-114.

96. Roozbeh Jafari, Foad Dabiri, Philip Brisk, and Majid Sarrafzadeh. "Adaptive and fault tolerant medical vest for life-critical medical monitoring," *20th ACM Symposium on Applied Computing (SAC)*, March, 2005, pp. 272-279.

97. Philip Brisk, Adam Kaplan, and Majid Sarrafzadeh. "Area efficient instruction set synthesis for reconfigurable system-on-chip designs," *41st Design Automation Conference (DAC)*, June, 2004, pp. 395-400.

98. Philip Brisk, Adam Kaplan, and Majid Sarrafzadeh. "Parallel analysis of the rijndael block cipher," *IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS)*, November, 2003.

99. Adam Kaplan, Philip Brisk, and Ryan Kastner. "Data communication estimation and reduction for reconfigurable systems," *40th Design Automation Conference (DAC)*, June, 2003, pp. 616-621.

100. Philip Brisk, Adam Kaplan, Ryan Kastner, and Majid Sarrafzadeh. "Instruction generation and regularity extraction for reconfigurable processors," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, September, 2002, pp. 262-269.

### *Workshops (Peer-reviewed, with proceedings)*

1. Maryam Shahcheraghi, Trevor Cappon, Samet Oymak, Evangelos Papalexakis, Eamonn Keogh, Zachary Zimmerman, and Philip Brisk. "Matrix Profile Index Prediction for Streaming Time Series," *Workshop on ML for Systems and NeurIPS*, December, 2020.

2. Jani Boutellier, Alessandro Cevrero, Philip Brisk, and Paolo Ienne. “Architectural support for the orchestration of fine-grained multiprocessing for portable streaming applications,” *IEEE Workshop on Signal Processing Systems (SiPS)*, October, 2009, pp. 115-120.
3. Francesco Regazzoni, Alessandro Cevrero, François-Xavier Standaert, Stephane Badel, Theo Kluter, Philip Brisk, Yusuf Leblebici, and Paolo Ienne. “A design flow and evaluation framework for DPA-resistant instruction set extensions,” *Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, September, 2009, pp. 205-219.
4. Jani Boutellier, Veeranjaneyulu Sadhanala, Christophe Lucarz, Philip Brisk, and Marco Mattavelli “Scheduling of dataflow models within the reconfigurable video coding framework,” *IEEE Workshop on Signal Processing Systems (SiPS)*, October, 2008, pp. 182-187.
5. Tammara Massey, Foad Dabiri, Roozbeh Jafari, Hyduke Noshadi, Philip Brisk, and Majid Sarrafzadeh. “Towards reconfigurable embedded medical systems,” *Workshop on High Confidence Medical Devices, Software, and Systems and Medical Device Plug-and-Play Interoperability (HCMDSS-MDPnP)*, June, 2007, pp. 178-180.
6. Philip Brisk and Majid Sarrafzadeh. “Interference graphs for procedures in static single information form are interval graphs,” *10th Workshop on Software and Compilers for Embedded Systems (SCOPES)*, April, 2007, pp. 101-110.
7. Philip Brisk, Ani Nahapetian, and Majid Sarrafzadeh. “Instruction selection for compilers that target architectures with echo instructions,” *8th International Workshop on Software and Compilers for Embedded Systems (SCOPES)*, September, 2004, pp. 229-243.

### *Workshops/Posters (Peer-reviewed, without proceedings)*

1. Radhakrishna Sanka, Brian Crites, Joshua Lippai, Jeffrey McDaniel, Philip Brisk, and Douglas Densmore. “Standardizing design performance comparison in microfluidic manufacturing,” *International Workshop on Biological Design Automation (IWBDA)*, Berkeley, CA, USA, July-August 2018.
2. Brian Crites, Jeffrey McDaniel, Heran Bhakta, William Grover, and Philip Brisk. “Design tools for microfluidic devices,” *International MicroNano Conference*, December, 2017.
3. Brian Crites, Karen Kong, and Philip Brisk. “Diagonal component expansion for flow-layer placement of flow-based microfluidic biochips,” *54th Design Automation Conference (DAC), Work-in-Progress (WIP) Session*, June, 2017.
4. Hadi Parandeh-Afshar, Grace Zgheib, Philip Brisk, and Paolo Ienne. “Routing wire optimization through generic synthesis on FPGA carry chains,” *20th International Workshop on Logic and Synthesis (IWLS)*, June 2011, pp. 129-135.
5. Hadi Parandeh-Afshar, Arkosnato Neogy, Philip Brisk, and Paolo Ienne. “Improved synthesis of compressor trees on FPGAs by a hybrid and systematic design approach,” *19th International Workshop on Logic and Synthesis (IWLS)*, June, 2010, pp. 193-200.
6. Ajay K. Verma, Philip Brisk, and Paolo Ienne. “A decomposition algorithm to structure arithmetic circuits,” *18th International Workshop on Logic and Synthesis (IWLS)*, July, 2009.
7. Ajay K. Verma, Philip Brisk, and Paolo Ienne “$XP^2$: a new compact representation for manipulating arithmetic circuits,” *17th International Workshop on Logic and Synthesis (IWLS)*, June, 2008.
8. Philip Brisk, Ajay K. Verma, and Paolo Ienne. “Optimal polynomial-time interprocedural register allocation for high-level synthesis using SSA Form,” *16th International Workshop on Logic and Synthesis (IWLS)*, June, 2007.
9. Philip Brisk, Ajay K. Verma, Paolo Ienne, and Majid Sarrafzadeh. “Interconnect optimization for high-level synthesis of static single assignment form programs (poster),” *16th International Workshop on Logic and Synthesis (IWLS)*, June, 2007.
10. Philip Brisk and Majid Sarrafzadeh. “Static single assignment form and the dominance relation (poster),” *16th International Workshop on Logic and Synthesis (IWLS)*, June, 2007.

11. Philip Brisk, Foad Dabiri, Jamie Macbeth, and Majid Sarrafzadeh. "Polynomial-time graph coloring register allocation," *14th International Workshop on Logic and Synthesis (IWLS)*, June, 2005.
12. Ryan Kastner, Wenrui Gong, Xin Hau, Forrest Brewer, Adam Kaplan, Philip Brisk, and Majid Sarrafzadeh. "Physically aware data communication optimization for hardware synthesis," *14th International Workshop on Logic and Synthesis (IWLS)*, June, 2005.
13. Philip Brisk and Majid Sarrafzadeh. "Framework and design methodology for a compiler that compresses code using echo instructions," *2nd Workshop on Optimization for DSP and Embedded Systems (ODES-2)*, March, 2004.

### *Posters (Abstract-only)*

1. Sina Faezi, Sujit Rokka Chhetri, Arnav Vaibhav Malawade, John Charles Chaput, William H. Grover, Philip Brisk, and Mohammad Abdullah Al Faruque. "Acoustic side channel attack against DNA synthesis machines: poster abstract" *International Conference on Cyber-Physical Systems (ICCPS) Work-in-Progress Session*, April, 2020.
2. Alessandro Cevrero, Panagiotis Athanasopoulos, Hadi Parandeh-Afshar, Maurizio Skerlj, Philip Brisk, Yusuf Leblebici, and Paolo Ienne. "3D configuration caching for 2D FPGAs (poster)," *17th International Symposium on FPGAs (FPGA)*, February, 2009, p. 286

### *Technical Reports*

1. Benoit Boissinot, Philip Brisk, Alain Darte, and Fabrice Rastello. "SSI Revisited," Technical Report LIP-2009-24, ENS-Lyon, 2009.

## Patents

1. Philip Brisk, Brian Crites, Jeffrey McDaniel. Microfluidics Planar Placement and Routing Algorithm. US Pat. 10,360,336. Issue date 7/23/19.

## Invited Talks

- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," Personal Biochips – Summer Workshop, ATLAS Institute, University of Colorado, Boulder, July 22-26, 2019.
- "Exact Time Series Motif Discovery using a Commercial GPU Cluster: How to Execute More than One Quintillion Pairware Comparisons in a Single Day," Pompeu Fabra University, Barcelona, Spain, June 18, 2019.
- "Acoustic Time Series in Industry 4.0: Improved Reliability and Cyber-Security Vulnerabilities," *J on the Beach*, Marbella, Spain, May 16, 2019.
- "Programmable Microfluidics: Automating Life Science, Health, and Medical Research," *Workshop on Advanced Topics in Computing*, University of Lugano, Switzerland, October 26, 2018.
- "Hardware-Accelerated Time-Series Data Mining Algorithms," Hong Kong City University, Kong Kong SAR, China, July 11, 2018.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," The University of Hong Kong, Hong Kong SAR, China, July 11, 2018.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," University of Tennessee, Knoxville, TN, USA, June 7, 2018.

- "Predictive Performance Modeling for Integrated Graphics Accelerators," Georgia Institute of Technology, Atlanta, GA, USA, June 4, 2018.
- "Hardware-Accelerated Time-Series Data Mining Algorithms," EPFL, Switzerland, May 30, 2018.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," EPFL at Microcity, Neuchâtel, Switzerland, May 28, 2018.
- "Language and Compiler Design for Laboratories-on-a-Chip," ENS-Paris, France, March 22, 2018.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," Technical University of Vienna, Vienna, Austria, March 1, 2018.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," Johannes Kepler University, Linz, Austria, February 26, 2018.
- "Advances in Modeling and Simulation for Microfluidics," MF-9.2, Ninth Microfluidics Consortium, San Jose, CA, USA, February 1, 2018.
- "Language and Compiler Design for Laboratories-on-a-Chip," ETH Zurich (Luca Benini Group), Switzerland, December 20, 2017.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," ETH Zurich (Andrew deMello Group), Switzerland, December 19, 2017.
- "Language and Compiler Design for Laboratories-on-a-Chip," EPFL, Switzerland, December 18, 2017.
- "Design Software for Microfluidics: Integrating Fluid Modeling with Design Objectives," University of Twente, Enschede, The Netherlands, December 14, 2017.
- "Language and Compiler Design for Laboratories-on-a-Chip," Delft University of Technology, The Netherlands, December 12, 2017.
- "Computer-Assisted Modeling and Simulation for Microfluidics: Progress and Challenges," MF-9.1, Ninth Microfluidics Consortium, Amsterdam, The Netherlands, December 11, 2017.
- "Predictive Performance Modeling for Integrated Graphics Accelerators," University of Amsterdam, The Netherlands, December 11, 2017.
- "Physical Design Automation for Microfluidic Large Scale Integration Biochips," CMOS Emerging Technologies Symposium, Warsaw, Poland, May 28-30, 2017.
- "Microfluidics and Biological Instrument Design as a Computing Discipline: An Overview," Johannes Kepler University, Linz, Austria, May 16, 2017.
- "Microfluidic Design Tools, MECs, Standardization, and other Unsolicited Commentary," MF-8.3, Eighth Microfluidics Consortium, Zurich, Switzerland, April 4-5, 2017.
- "Customizable processor acceleration of time series similarity search for the Internet of Things," *Workshop on VLSI for IoT*, co-located with Design *Automation and Test in Europe (DATE)*, Lausanne, Switzerland, March 31, 2017.
- "Keynote: Recent developments in microfluidic large scale integration," Semiconductor Research Corporation (SRC) Workshop on Electronic Design Automation (EDA)/Biological Design Automation (BDA) Interaction Roadmap, Newcastle upon Tyne, UK, August 19-20, 2016.
- "Programmable, integrated microfluidic technology: automating and miniaturizing chemistry and biochemistry," CMOS Emerging Technologies Research Symposium, Vancouver, BC, Canada, May 20-22, 2015
- "Programming languages, compilers, and synthesis/VLSI tools for microfluidics," University of British Columbia, May 20, 2015

- "Software control of cyber-physical electrowetting devices," 9th International Meeting on Electrowetting and Related Micro/Electrofluidic Science and Technology, Cincinnati, OH, June 23-25, 2014
- "An application-specific processor for real-time medical monitoring," Friedrich-Alexander-Universität Erlangen-Nürnberg, March 21, 2014
- "Laboratories-on-a-chip: the application of computer engineering principles to biochemistry," Friedrich-Alexander-Universität Erlangen-Nürnberg, March 19, 2014
- "Laboratories-on-a-chip: the application of computer engineering principles to biochemistry," 3rd Workshop of the DFG Research Training Group 1773 "Heterogeneous Image Systems", Obertrubach, Germany, March 17, 2014
- "The evolution of software-programmable cyber-physical digital microfluidic laboratories-on-a-chip," 2014 NSF Workshop on Research Frontiers in Medical Cyber-Physical Systems, Arlington, VA, USA, February 6-7, 2014
- "Laboratories-on-a-chip: the application of computer engineering principles to biochemistry," Ecole Polytechnique Fédérale de Lausanne (EPFL), January 24, 2014.
- "Laboratories-on-a-Chip: the application of computer engineering principles to biochemistry," University of California, Irvine, October 11, 2013
- "Laboratories-on-a-Chip: the application of computer engineering principles to biochemistry," Nanyang Technical University, Singapore, August 30, 2013
- "Laboratories-on-a-Chip: the application of computer engineering principles to biochemistry," National University of Singapore, Singapore, August 27, 2013
- "Programmable, integrated microfluidic technology: automating and miniaturizing chemistry and biochemistry," (Interactive Tutorial) Design Automation Summer School, June 2-3, 2013 (co-located with the Design Automation Conference)
- "Laboratories-on-a-Chip: the application of computer engineering principles to biochemistry," Engineer's Week (E-Week), California State University, Northridge, February 19, 2013
- "Feedback-driven assay interpretation using digital microfluidic biochips," Third Annual NSF CPS PI Meeting, National Harbor, MD, October 4, 2012.
- "Routing algorithms for FPGAs with sparse intra-cluster routing crossbars," Microsemi Corporation, San Jose, CA, September 20, 2012.
- "Reducing the cost of floating-point mantissa alignment and normalization in FPGAs," Peking University / UCLA Center for Energy-efficient Computing and Applications (CECA), Beijing, China, September 13, 2012.
- "Programmable microfluidics: why the biochemist of the future will be a programmer," Department of Computer Science and Engineering, University of California, San Diego, October 11, 2011.
- "Toward programmable droplet-based microfluidic laboratories-on-chip," Riverside Technology CEO Forum, July 5, 2011 (presented by Daniel Grissom)
- "Architecture and design Automation for ASIPs," Design Automation Summer School (Colocated with the Design Automation Conference), June 5-6, 2011.
- "Programmable microfluidics: why the biochemist of the future will be a programmer, and why the PL&S community should lead the way," Southern California Workshop on Programming Languages and Systems, Harvey Mudd College, April 16, 2011 (with Daniel Grissom)
- "Overview of the reconfigurable video coding framework," IGERT on Video Bioinformatics, University of California, Riverside, April 1, 2011.
- "Programmable laboratories-on-chip: why the biochemist of the future will be a programmer," Department of Electrical Engineering, University of California, Riverside, February 28, 2011.

- "Microfluidics technology," Riverside Technology CEO Forum, December 7, 2010. "Improving FPGA Performance for Carry-save Arithmetic," Department of Computer Science, University of California, Los Angeles, November 23, 2009.
- "Low-cost coherence solutions for application-specific processors with custom instruction set extensions that access local memories," Department of Computer Science and Engineering, University of California, Riverside, October 19, 2009.
- "The landscape of SSA-based program representations." Static Single Assignment Form Seminar. Autrans, France, April 27-30, 2009.
- "Improving FPGA performance for carry-save arithmetic," Department of Electrical and Computer Engineering, University of Waterloo, April 8, 2009. (Faculty candidate interview)
- "Improving FPGA Performance for carry-save arithmetic," Department of Electrical and Computer Engineering, George Washington University, April 1, 2009. (Faculty candidate interview)
- "Improving FPGA performance for carry-save arithmetic," Department of Electrical and Computer Engineering, University of British Columbia, March 26, 2009.
- "Improving FPGA performance for carry-save arithmetic,' Department of Computer Science and Engineering, University of California, Riverside, March 2, 2009. (Faculty candidate interview)
- "Improving arithmetic performance for arithmetic circuits," Department of Computer Engineering, University of California, Santa Barbara, February 28, 2008.
- "Rethinking ISE identification: a new processor-agnostic method," Chair for Embedded Systems, Universitat Karlsruhe, October 18, 2007.

## Tutorials

- Janna Doppa and Philip Brisk, Machine Learning for Design and Optimization of Embedded Systems. Presented at Embedded Systems Week (ESWeek), October, 2019.
- Florent Bouchez, Philip Brisk, Sebastian Hack, Jens Palsberg, and Fabrice Rastello, SSA based Register Allocation. Presented at thes International Workshop on Language and Compilers for Parallel Computing (LCPC), October, 2009.
- Philip Brisk, Alain Darte, Sebastian Hack, Jens Palsberg, and Fabrice Rastello, SSA-based Register Allocation. Presented at the International Symposium on Code Generation and Optimization (CGO), March, 2009.
- Philip Brisk, Alain Darte, Sebastian Hack, Jens Palsberg, Fernando M. Q. Pereira, and Fabrice Rastello, SSA-based Register Allocation. Presented at conjunction with Embedded Systems Week, October, 2008.

## Professional Activities

### *Organizing Committees*

- Co-Chair, System Design Contest, *Design Automation Conference (DAC)*, 2020
- Co-Chair, System Design Contest, *Design Automation Conference (DAC)*, 2019
- Finance Chair, *28th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, 2017
- Program Co-Chair, *26th International Conference on Field Programmable Logic and Applications (FPL)*, 2016
- Finance Chair, *21st ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2013
- Program Co-Chair, *9th International Symposium on Applied Reconfigurable Computing (ARC)*, 2013

- Publicity Chair, *8th International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC)*, 2013
- Topic Co-Chair: T11. Logic and high-level synthesis, SW synthesis, HW-SW co-design *20th IEEE/IFIP International Conference on Very Large Scale Integration and System-on-a- Chip (VLSI-SoC)*, 2012
- Program Chair, *20th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2012
- Publicity Chair, *7th International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC)*, 2012
- Finance Chair, *22nd IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, 2011
- Program co-Chair, *9th IEEE Symposium on Application-Specific Processors (SASP)*, 2011
- General Chair, *19th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2011
- Student Travel Grant Chair, *16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2011
- General co-Chair, *8th IEEE Symposium on Application-Specific Processors (SASP)*, 2010
- Special Session Chair, *18th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)* 2010
- General co-Chair, *4th IEEE Symposium on Industrial Embedded Systems (SIES)*, 2009
- Publicity Chair, *7th IEEE Symposium on Application-Specific Processors (SASP)*, 2009
- Local Arrangements Chair, *6th IEEE Symposium on Application-Specific Processors (SASP)*, 2008

## *Technical Program Committees*

- *Design Automation and Test in Europe (DATE)* 2021, PhD Forum
- *29th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2021*
- *12th ACM/IEEE International Conference on Cyber-Physical Systems (ICCPS), 2021*
- *29th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2021
- *26th Asia and South Pacific Design Automation Conference (ASPDAC)*, 2021, Embedded Systems Software Track (Track Chair)
- *International Conference on Field Programmable Technology (ICFPT)* 2020
- *30th International Conference on Field Programmable Logic and Applications (FPL)*, 2020
- *30h Great Lakes Symposium on VLSI (GLS-VLSI)* 2020, Track: VLSI for Machine Learning and Artificial Intelligence
- *Design Automation and Test in Europe (DATE)* 2020, PhD Forum
- *Design Automation and Test in Europe (DATE)* 2020, Track D11, Reconfigurable Computing (Track Co-Chair)
- *28th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2020*
- *28th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2020
- *International Conference on Field Programmable Technology (ICFPT)* 2019
- *30th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, 2019
- *29th International Conference on Field Programmable Logic and Applications (FPL)*, 2019

- *22nd Euromicro Conference on Digital System Design (DSD)* 2019, Special Session: Future Trends in Emerging Technologies (FTET)
- *Design Automation Conference (DAC)*, 2019; Late-breaking Results
- *Design Automation Conference (DAC)*, 2019; Track: ESS2, Embedded System Design Methodologies (Track Co-Chair)
- *29h Great Lakes Symposium on VLSI (GLS-VLSI)* 2019, Track: VLSI for Machine Learning and Artificial Intelligence (Track Co-Chair)
- *27th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2019
- *International Conference on Field Programmable Technology (ICFPT)* 2018
- *Design Automation and Test in Europe (DATE)* 2019, Track D11, Reconfigurable Computing (Track Co-Chair); Best Paper Award Committee.
- *International Conference on Computer-Aided Design (ICCAD)* 2018, Track 4.1, Biological Systems and Electronics, Brain Inspired Computing, and New Computing Paradigms (Track Chair)
- *29th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, 2018
- *28th International Conference on Field Programmable Logic and Applications (FPL)*, 2018
- *21st Euromicro Conference on Digital System Design (DSD)* 2018, Special Session: Future Trends in Emerging Technologies (FTET)
- *28th Great Lakes Symposium on VLSI (GLS-VLSI)* 2018, Track: VLSI for Machine Learning and Artificial Intelligence (Track Co-Chair)
- *Design Automation and Test in Europe (DATE)* 2018, Track A7, Applications of Emerging Technologies, and Track D11, Reconfigurable Computing
- *26th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2018
- *International Conference on Field Programmable Technology (ICFPT)* 2017
- *28th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, 2017
- *27th International Conference on Field Programmable Logic and Applications (FPL)*, 2017
- *International Conference on Computer-Aided Design (ICCAD)* 2017
- *27th Great Lakes Symposium on VLSI (GLS-VLSI)*, Track 7: Biochips and Biological Systems
- *25th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2017
- *Design Automation and Test in Europe (DATE)* 2017, Track D11, Reconfigurable Computing (Topic Co-Chair)
- *International Conference on Field Programmable Technology (ICFPT)* 2016
- *International Conference on Computer-Aided Design (ICCAD)* 2016, Track 1.6, Design issues for Heterogeneous Computing & Cloud Computing
- *25th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)* 2016
- *International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)*, 2016
- *Design Automation Conference (DAC)*, 2016; Track EDA1, System-on-chip design and HW/SW codesign
- *24th International Symposium on Field Programmable Gate Arrays (FPGA)*, 2016
- *Design Automation and Test in Europe (DATE)* 2016, Track D11, Reconfigurable Computing

- *11th International Conference on High Performance Embedded Architecture and Compilers (HiPEAC):* Member: Board of Distinguished Reviewers, 2016
- *International Conference on Field Programmable Technology (ICFPT)* 2015
- *25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015
- *Design Automation Conference (DAC)*, 2015; Track EDA1, System-on-chip design and HW/SW codesign
- *18th Euromicro Conference on Digital System Design (DSD)*; Special Session on Emerging Technologies and Circuit Synthesis (ETCS), 2015
- *24th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2015
- *16th International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2015
- *23rd International Symposium on Field Programmable Gate Arrays (FPGA)*, 2015
- *Design Automation and Test in Europe (DATE)* 2015, Track D11, Reconfigurable Computing
- *10th International Conference on High Performance Embedded Architecture and Compilers (HiPEAC):* Member: Board of Distinguished Reviewers, 2015
- *International Conference on Field Programmable Technology (ICFPT)* 2014
- *22nd International Conference on Very Large Scale Integration (VLSI-SoC)* 2014, Track on Hardware/Software Codesign
- *24th International Conference on Field Programmable Logic and Applications (FPL)*, 2014
- *17th Euromicro Conference on Digital System Design (DSD)*; Special Session on Emerging Technologies and Circuit Synthesis (ETCS), 2014
- *23rd ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2014
- *15th International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2014
- *Design Automation Conference (DAC)*, 2014; Track EDA1, System-on-chip design and HW/SW codesign
- *Design Automation and Test in Europe (DATE)* 2014, Track D6, Emerging Technologies, Systems, and Applications
- *19th Asia and South Pacific Design Automation Conference (ASPDAC)* 2014, Track 4, Embedded and Real-time Systems
- *9th International Conference on High Performance Embedded Architecture and Compilers (HiPEAC)* 2014 Member: Board of Distinguished Reviewers, 2014
- *International Conference on Field Programmable Technology (ICFPT)* 2013
- *21st International Conference on Very Large Scale Integration (VLSI-SoC)* 2013, Track T9 on Reconfigurable, Adaptive, FPGA
- *23rd International Conference on Field Programmable Logic and Applications (FPL)*, 2013
- *8th IEEE Symposium on Industrial Embedded Systems (SIES)*, 2013
- *9th International Wireless Communication and Mobile Computing Conference (IWCMC)*, 2013
- *14th International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2013
- *4th International Workshop on Highly Efficient Accelerators and Reconfigurable Technology (HEART)*, 2013
- *26th International Conference on Architecture of Computing Systems (ARCS)*, 2013

- *18th Asia and South Pacific Design Automation Conference (ASPDAC)*, 2013. Subcommittee on Embedded and Real-time Systems, and Best Paper Award Subcommittee
- *8th International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC)*; Member: Board of Distinguished Reviewers, 2013
- *International Conference on Field-Programmable Technology (ICFPT)*, 2012
- *7th IEEE Symposium on Industrial Embedded Systems (SIES)*, 2012
- *3rd International Workshop on Highly Efficient Accelerators and Reconfigurable Technology (HEART)*, 2012
- *8th International Wireless Communication and Mobile Computing Conference (IWCMC)*, 2012
- *Design Automation and Test in Europe (DATE)*, 2012 Track D10 on Architecture and High-level Synthesis
- *25th International Conference on Architecture of Computing Systems (ARCS)*, 2012
- *7th International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC)*; Member: Board of Distinguished Reviewers, 2012
- *3rd International ICST Conference on Mobile Computing, Applications, and Services (MOBICASE)*, 2011
- *6th IEEE Symposium on Industrial Embedded Systems (SIES)*, 2011
- *24th International Conference on Architecture of Computing Systems (ARCS)*, 2011
- *Design Automation and Test in Europe (DATE)*, 2011, Track D10 on Architectural and High-level Synthesis
- *5th IEEE Symposium on Industrial Embedded Systems (SIES)*, 2010
- *17th Reconfigurable Architecture Workshop (RAW)*, 2010
- *Design Automation and Test in Europe (DATE)*, 2010, Track D11 on Architectural and High-level Synthesis
- *23rd International Conference on Architecture of Computing Systems (ARCS)*, 2010
- *16th Reconfigurable Architecture Workshop (RAW)*, 2009
- *6th IEEE Symposium on Application-Specific Processors (SASP)*, 2008
- *11th International Workshop on Software and Compilers for Embedded Systems (SCOPES)*, 2008
- *5th Workshop on Application-Specific Processors (WASP)*, 2007

## *Session Chair:*

- "Special Session 11: Attacking Dynamic Optimizations in the Era of Complex Heterogeneous Multi-core Computing I," *International Symposium on VLSI (ISVLSI)*, 2018
- "Younger, Faster, and More Connected," *54th Design Automation Conference (DAC)*, 2017
- "High Performance Reconfigurable Computing," *Design Automation and Test in Europe (DATE)*, 2017
- "The Coming Age of Microfluidics: EDA Solutions for Enabling Biochemistry on a Chip!," *51st Design Automation Conference (DAC)*, 2014
- "To Remember or Not: Embedded Memories," *31st International Conference on Computer-Aided Design (ICCAD)*, 2013
- "Answers to Some of Your Embedded Systems Design Questions," *50th Design Automation Conference*, 2013
- "Applications (I)," *9th International Symposium on Applied Reconfigurable Computing (ARC)*, 2013

- "Memory and Storage Management," *18th Asia and South Pacific Design Automation Conference (ASPDAC)*, 2013
- "Computational Approaches for Biological Systems," *30th International Conference on Computer-Aided Design (ICCAD)*, 2012
- "Multi-core and Embedded SoC," *20th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2012
- "Adaptive Computing: When, Where, Why, How," *49th Design Automation Conference (DAC)*, 2012
- "Testing, Reliability, and Fault Tolerance (I)," *9th IEEE International Conference on ASIC (ASICON)*, 2011
- "Computing Fabrics: Cores, LUTs, and Molecules," 4*8th Design Automation Conference (DAC)*, 2011
- "Advances in Core Logic Synthesis," *International Conference on Computer- Aided Design (ICCAD)*, 2010
- "Logic Synthesis is Alive and Kicking," *47th Design Automation Conference (DAC)*, 2010.
- "Leveraging Parallelism in FPGAs and Multicore Systems," *46th Design Automation Conference (DAC)*, 2009
- "Validation and Simulation," *11th International Workshop on Software and Compilers for Embedded Systems (SCOPES)*, 2008
- "High-level Synthesis and IP Protection," *Design Automation and Test in Europe (DATE)*, 2008
- "Applications," *5th Workshop on Application-Specific Processors (WASP)*, 2007

## *Associate Editor:*

- IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD), **2018-present**
- Integration: The VLSI Journal (Elsevier), **2011-present**
- Guest Editor: IET Cyber-Physical Systems: Theory & Applications
- Guest Editor: ACM Transactions on Embedded Computing Systems (TECS)
  Special Issue on Application Specific Processors 13(2), September, 2013.

## *Anonymous Referee:*

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computers (TCOMP)
- IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
- IEEE Transactions on Industrial Informatics (TII)
- IEEE Transactions on Biomedical Circuits and Systems (TBCAS)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Transactions on Automation Science and Engineering (T-ASE)
- IEEE Transactions on Multi-Scale Computing Systems (TMSCS)
- IEEE Embedded Systems Letters (ESL)
- IEEE Design & Test
- IEEE Micro
- IEEE Communications Magazine

- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Architecture and Code Optimization (TACO)
- ACM Transactions on Design Automation for Electronic Systems (TODAES)
- ACM Computing Surveys (CSUR)
- Transactions on High Performance Embedded Architectures and Compilers (HiPEAC)
- Microfluidics and Nanofluidics
- Microelectronics Journal
- Micromachines
- Bioengineering
- Software: Practice and Experience
- IET Transactions on Computers and Digital Techniques
- IET Electronics Letters
- Integration: The VLSI Journal
- Journal of Systems Architecture
- International Journal of Reconfigurable Computing
- Journal of Computer Science and Technology
- Springer Journal on Design Automation for Embedded Systems (DAEM)
- Quantum Information Processing
- Mobile Networks and Applications

## Current Students

### *Ph.D.*

- Lisa Chen
- Chad Davies
- Mariana Duarte
- Yilmaz Serhan Gener
- Amir Hosseinian
- Amin Kalantar
- Tyson Loveless
- Jason Mandala (EE)
- Jonathan Meyer
- Phillip Park
- Joshua Potter
- Javad Saber-Latibari (co-advised with M. Lesani)
- Maryam Shahcheraghi
- Daniel Tan

### *M.S.*

- Rogelio Macedo
- Prithviraj Yuvaraj

*Undergraduate Student Researchers*

- Christopher Alexman
- Ratnodeep Bandyopadhyay
- Julian Beaulieu
- Trevor Cappon
- Sabrina Carlos
- Aaron Chen
- Tandy Dang
- Christopher de la Torre
- Helen Du
- Arya Faramarzi
- Alex K. Fay (Pomona College)
- Valeria Garibaldi
- Saul Gonzalez
- Ryan Hu
- Suhas Jagannath
- Quinn Leader
- Sana Mohiuddin
- Ruth Navarette
- Marios Nicolaides
- Alejandro Sherman
- Xianghu Wang (UCR GPP Program)

## Alumni and Past Students (UC Riverside)

*Ph.D.*

- Syed Md. Jaffrey Al-Kadry (Spring, 2012)
  "A power-reduction technique through dynamic runtime algorithm for CMOS VLSI circuits"
  First Employment: GM Hybrid-Electric Vehicles Group
- Daniel Grissom (Spring, 2014)
  "Design of Topologies for Interpreting Assays on Digital Microfluidic Biochips"
  First Employment: Azusa Pacific University
- Yehdhih Ould Mohammed Moctar (Spring, 2014)
  "Parallel Routing for Field Programmable Gate Arrays with Sparse Intra-Cluster Routing Crossbars"
  First Employment: IBM
- Jeffrey McDaniel (Summer 2016)
  "Design Automation of Continuous Flow-Based Microfluidic Biochips"
  First Employment: UCR Lecturer / Entrepreneur
- Kenneth O'Neal (Spring 2018)
  "Performance and Power Prediction of Compute Accelerators Using Machine Learning"
  First Employment: Intel Corporation
- Brian Crites (Spring 2018)
  "Placement, Routing, and Post-processing of Microfluidic Device Flow-Layers"
  First Employment: Bird Corporation
- Jason Ott (Fall 2019)
  "Programming Safe Chemistry on Laboratories-on-a-Chip"
  First Employment: Oracle
- Zachary Zimmerman (Fall 2019)
  "Breaking Computational Barriers to Perform Time Series Pattern Mining at Scale and at the Edge"

First Employment: Google

*M.S.*

- Eric Clay (Fall, 2015)
- Brian Crites (Fall, 2014)
- Christopher Curtis (Winter, 2016)
- Daniel Grissom (Summer, 2011)
- Ian Hodgkinson (Spring, 2014)
- Yeshwanth Kallati (Winter 2021)
- Mohammed Khorramzadeh (Spring, 2014)
- Navin Kumar (Winter, 2014)
- Jacob Leung (Fall, 2011)
- Mark Louton (Spring, 2013)
- Andrew Lvovsky (Summer 2020)
- Deen Ma (Summer, 2015)
- Jeffrey McDaniel (Spring, 2014)
- Pavithra Murali (Summer, 2013)
- Kenneth O'Neal (Winter, 2016)
- Richard Ramos (Fall, 2011)
- James Robinson (Spring, 2015)
- Alex Rogers (Fall, 2015)
- Ben Sanders (Spring, 2013)
- Aditya Tammewar (Spring, 2014)
- Joseph Tarango (Spring, 2013)

*Undergraduate*

- Victoria Albezer (2020)
- Christian Alvarado (2019)
- Carlos Avila (2010)
- Auralila Baez (2011-2013)
- Gregory Bailey (2011-2012)
- Neesha Bhardwaj (2017-2018)
- Rick Boshae (2016)
- Michael Bradley (2018-2019)
- Adriel Bustamante (2018-2019)
- Jiahe Cao (UCR GPP Program) (2019-2020)
- Hsin-Yu (Cindy) Fan Chiang (2016-2017)
- Brian Crites (2011-2012)
- Christopher Curtis (2011-2014)
- Alexander Dela Cruz (2019-2020)
- Kennen Derenard (2017-2019)
- Edward Dickhoff (2018-2019)
- Robert Doherty (2012)
- Cody Falzone (2017-2018)
- Jonathan Fiske (2011-2014)
- Aaron Sigal (2019-2020)
- Aaron Gonzales (2013-2014)
- Andrew Gwozdziowski (2011-2013)
- Christopher Hansen (Azusa Pacific University) (2016-2017)
- Emily Huang (2018)
- Janine Huang (2017-2018)

- Jordan Ishii (Azusa Pacific University (2016-2017)
- Christopher Jaress (2013-2014)
- Timothy Johnsen (Riverside Community College/UC Irvine) (2014)
- Karen Kong (2016-2018)
- Chun "Johnnie" Kwok (2010-2012)
- Jesse Layman (2016-2018)
- Alic Lien (2018-2020)
- Mitch Liu (2016-2017)
- Steven Lopez (2016-2017)
- Tristan Lopez (2019-2020)
- Tyson Loveless (2016-2017)
- James Luo (2017-2018)
- Andrew Lvovsky (2019)
- Joel Lwanga (2014)
- Rogelio Macedo (2019-2020)
- Valeed Malik (2013)
- Otitochi "Tito" Mbagwu (MIT) (2011)
- Jeffrey McDaniel (2010-2011)
- Jonathan Meyer (2019-2020)
- Faith Mwiza (Cal Baptist) (2011)
- Andrew Nava-Juarez (2015-2017)
- Christopher Nguyen (2019-2020)
- Matthew Nichols (2011-2012)
- Kenneth O'Neal (2011-2012)
- Dylan O'Neill (2015-2017)
- Natasha Orie (2017-2018)
- Phillip Park (2018)
- Brendon Parker (2013)
- Hiral Patel (2012)
- Calvin Phung (2011-2012)
- Ian Pollard (Cal Poly. Pomona) (2016)
- Benjamin Preciado (2012)
- Stephanie Qian (2018-2019)
- Arvel Reeves (2019-2020)
- Sean Richardson (2019)
- Samantha Robinson (2016-2018)
- Mat Schaffrath (2016-2018)
- Siddhanth Sharma (2019-2020)
- Tom Shih (2019)
- Aaron Sigal (2019-2020)
- Nikita Singh (2017-2018)
- Olivia Smith (2016)
- Aditya Tammewar (2011-2012)
- Hans Tang (2016-2018)
- Kevin Tang (2018-2019)
- Joseph Tarango (2010)
- Hongzhen Tian (UCR GPP Program) (2019-2020)
- Ulyana Tkachenko (2017-2018)
- Jimmy Tran (2015-2016)
- Uy Tran (2018-2020)
- Vinh-Trung Trinh (2018-2019)
- Yesenia Vital (2011)
- Erin Wong (2018-2019)

- Tyler Woods (2019-2020)
- Alberto Tam Yong (2015)
- Zachary Zimmerman (2014-2015)

*External MS Thesis Supervision*

- Christian Kohn (Freidric-Alexander-Universitat Erlangen-Nurnberg) (2010)
  "Input Interconnect Block to Integrate a Field Programmable Compressor Tree into a Field Programmable Gate Array"

## Alumni and Past Students (EPFL)

*MS Thesis Supervision*

- Alessandro Cevrero (EPFL) (2007)
  Thesis: "Exploring new architectures for reconfigurable hardware"
- Nithin George (Technical University of Munich) (2009)
  Thesis: "Optimizing FPGA routing networks for improved floating-point performance"
- Hosein Seyed Attarzadeh Niaki (KTH) (2008)
  Thesis: "Design space exploration of field programmable counter arrays and their integration into FPGAs"
- Pascal Plancherel (EPFL) (2009)
  Thesis: "Logarithmic arithmetic unit"

*MS Semester Project Supervision*

- Ioannis Sotiropoulos (EPFL) (2009)
  Project: "Hardware divider and logarithm unit for FPGA"
- Aanjhan Ranganathan (EPFL) (2009)
  Project: "Snoopy coherence energy reduction for embedded systems"
- Samuel Burri (EPFL) (2009)
  Project: "Ensuring coherence between an L1 cache and a scratchpad memory in an embedded system without using a coherence protocol"

*Internship Supervision (EPFL)*

- Jani Boutellier (University of Oulu) (2007-2008)
- Arun Paidimarri (Indian Institute of Technology, Bombay) (2008)
- Hadi Parandeh-Afshar (University of Tehran) (2007)
- Nagaraju Pothineni (Indian Institute of Technology, Delhi) (2007)
- Amit Verma (Indian Institute of Technology, Kanpour) (2009)
- Yi Zhu (UCSD) (2007)
  Marcela Zuluaga (University of Edinburgh) (2008-2009)

## Teaching Experience

*UC Riverside*

| | |
|---|---|
| Spring 2021 | CS 220 Synthesis of Digital Systems (Graduate) |
| Winter 2021 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Fall 2020 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Summer 2020 | CS 179J Design Project in Computer Architecture and Embedded Systems (Undergraduate) |

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|---|---|
| Spring 2020 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Winter 2020 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Fall 2019 | CS 220 Synthesis of Digital Systems (Graduate) |
| Spring 2019 | CS 179J Design Project in Computer Architecture and Embedded Systems (Undergraduate) |
| Winter 2019 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 269 Seminar: Software and Hardware Engineering of Embedded Systems (Graduate/seminar) |
| Fall 2018 | CS 220 Synthesis of Digital Systems (Graduate) |
| Summer 2018: | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 175 Entrepreneurship in Computing (Undergraduate) |
| Spring 2018: | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 269 Seminar: Software and Hardware Engineering of Embedded Systems (Graduate/seminar)<br>CS 302 Teaching Apprentice Practicum (Graduate/seminar |
| Winter 2018: | CS 302 Teaching Apprentice Practicum (Graduate/seminar) |
| Fall 2017 | CS 220 Synthesis of Digital Systems (Graduate)<br>CS 302 Teaching Apprentice Practicum (Graduate/seminar) |
| Summer 2016 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 193 Design Project (Undergraduate) |
| Spring 2016 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Winter 2016 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Summer 2015 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 193 Design Project (Undergraduate) |
| Spring 2015 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 190 Special Studies (Undergraduate) |
| Winter 2015 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Summer 2015 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 193 Design Project (Undergraduate) |
| Winter 2015 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Fall 2014 | CS 141 Intermediate Data Structures and Algorithms<br>CS 220 Synthesis of Digital Systems (Graduate) |
| Summer 2014 | CS 179J Design Project in Computer Architecture and Embedded Systems (Undergraduate)<br>CS 193 Design Project (Undergraduate) |
| Spring 2014 | CS 223 Reconfigurable Computing (Graduate) |
| Winter 2014 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Fall 2013 | CS 161 Design and Architecture of Computer Systems (Undergraduate) |
| Spring 2013 | CS 220 Synthesis of Digital Systems (Graduate)<br>CS 287 Colloquium in Computer Science (Graduate/seminar) |
| Winter 2013 | CS/EE 120B Introduction to Embedded Systems (Undergraduate)<br>CS 287 Colloquium in Computer Science (Graduate/seminar) |
| Fall 2012 | CS 287 Colloquium in Computer Science (Graduate/seminar) |
| Spring 2012 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Winter 2012 | CS 179J Design Project in Computer Architecture and Embedded Systems (Undergraduate) |

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|---|---|
| Fall 2011 | CS 161 Design and Architecture of Computer Systems (Undergraduate)<br>CS 161L Design and Architecture of Computer Systems Laboratory (Undergraduate) |
| Spring 2011 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Winter 2011 | CS/EE 120B Introduction to Embedded Systems (Undergraduate) |
| Fall 2010 | CS 220 Synthesis of Digital Systems (Graduate) |
| Spring 2010 | CS 179J Design Project in Computer Architecture and Embedded Systems (Undergraduate) |
| Winter 2010 | CS 223 Reconfigurable Computing (Graduate) |

### *UCLA, Graduate Teaching Assistant*

- CS.M51A – Introduction to Digital Systems
- CS.132 – Compilers
- CS.M152A – Introductory Digital Design Lab
- CS.174 – Computer Graphics
- CS.180 – Algorithms and Complexity

## Outreach

### *Volunteer Mentoring and Judging*

- Science Fridays (SciFri), Crafton Hills College, Yucaipa, CA, February 20, and February 27, 2015
- Learning Computer Science through the Lens of Culture and Society ($LCS^2$) (Aprender la Informática por la Lente de la Cultura y la Sociedad) Crafton Hills College, Yucapia, CA, August 6, 2013
- Orange County Science and Engineering Fair, March 19, 2013, Costa Mesa, CA
- Intel ISEF Science Fair Regional Qualifying Competition, March 16, 2013, Irvine, CA
- Learning Computer Science through the Lens of Culture and Society ($LCS^2$) (Aprender la Informática por la Lente de la Cultura y la Sociedad) Crafton Hills College, Yucapia, CA, August 1, 2012
- Orange County Science and Engineering Fair, April 10, 2012, Costa Mesa, CA
- Intel ISEF Science Fair, Regional Qualifying Competition, March 31, 2012, Irvine, CA
- Los Angeles County Science Fair, March 29-30, 2012, Pasadena, CA
- Intel ISEF Science Fair, May 8-13, 2011, Los Angeles, CA
- Los Angeles County Science Fair, April 15, 2011, Pasadena, CA
- UC Riverside MESA (Mathematics, Engineering, and Science Achievement) Day Competition, February 26, 2011, Riverside, CA
- SACNAS – Society for Advancement of Chicanos and Native Americans in Science 2010 National Conference, September 30 – October 3, 2010, Anaheim, CA

### *Invited Talks*

- "My Career in Computer Science," Learning Computer Science through the Lens of Culture and Society ($LCS^2$) (Aprender la Informática por la Lente de la Cultura y la Sociedad) Crafton Hills College, Yucapia, CA, August 6, 2013
- "My Career in Computer Science," Learning Computer Science through the Lens of Culture and Society ($LCS^2$) (Aprender la Informática por la Lente de la Cultura y la Sociedad) Crafton Hills College, Yucapia, CA, August 1, 2012

### *UCR Advising*

- Faculty Advisor: IEEE at UCR (2012-2019)